Spring 4-1-2010

Digital Control Techniques for Single-Phase Power Factor Correction Rectifiers

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A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical, Computer and Energy Engineering

2010

This thesis entitled:
Digital Control Techniques for Single-Phase Power Factor Correction Rectifiers
written by Barry A. Mather
has been approved for the Department of Electrical, Computer and Energy Engineering

Professor Dragan Maksimović

Professor Regan Zane

Date

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Mather, Barry A. (Ph.D., Electrical Engineering)

Digital Control Techniques for Single-Phase Power Factor Correction Rectifiers

Thesis directed by Professor Dragan Maksimović

Tightening governmental regulations and industry standards for input current harmonics and input power factor correction (PFC) of common electronic devices such as servers, computers and televisions continues to increase the need for high-performance, low-cost power factor correction controllers. In response to this need, digital non-linear carrier (DNLC) PFC control has been developed and is presented in this thesis. DNLC PFC control offers many unique advantages over existing PFC control techniques in terms of design simplicity, low harmonic current shaping over a wide load range including CCM and DCM operation and a reliable, inexpensive digital implementation based on low-resolution analog-to-digital converters (A/D's) and digital pulse width modulator (DPWM). Implementation of the controller requires no microcontroller or digital signal processor (DSP) programming, and is well suited for a simple, low-cost integrated-circuit realization. DNLC PFC control is derived and analyzed for single-phase universal input PFC boost rectifiers. Further analysis of the operation of digitally controlled PFC rectifiers leads to the development of voltage loop compensator design constraints that avoid limit-cycling of the voltage loop. It is demonstrated that voltage loop limit-cycling is unavoidable when using traditional PFC control techniques under certain output loading conditions. However, it is also shown that voltage loop limit-cycling is avoidable under the same operating conditions when a DNLC PFC controller is implemented. Additionally, a unique output voltage sensing A/D is also developed that improves the PFC voltage loop transient response to load transients when paired with the DNLC PFC controller. Experimental results are shown for a 300W universal input boost PFC rectifier.

Acknowledgements

Thanks are due foremost to my advisor, Professor Dragan Maksimović, for teaching me how to perform research. His guidance and encouragement throughout my graduate studies have enhanced the entire learning experience. Thanks also to Professors Regan Zane and Robert Erickson for their excellent instruction in the areas of mixed-signal electronics and power electronics respectively.

Thank you to Professor Baylor Fox-Kemper for helping me improve my technical writing and reviewing skills. Professor Stanislaw Legowski, thank you for starting me down the path of graduate studies.

I would also like to acknowledge and thank Isaac Cohen and Larry Wofford of Texas Instruments for their continuous interest, support and advice regarding my research project.

Finally, I would like to thank my colleagues at the Colorado Power Electronics Center (CoPEC), my wife and my family for their patient help and gracious support.

Contents

Chapter

Tables

Table

Figures

Figure

Chapter 1

Introduction

The increasing pervasiveness and acceptance of household and personal electronic devices in recent years has created new challenges for switched-mode power supply (SMPS) designers in terms of cost, size and performance. For SMPS that operate off of the ac mains one particular set of performance specifications is the magnitude of the individual harmonic input currents above the fundamental. The undesirable effects of high harmonic input current content include increased RMS line currents limiting the power available to an ac load for a given ac service wire gauge, increased neutral currents in 3-phase systems, possible ac system instability and line voltage distortion. To mitigate these negative effects international standards such as EN 61000-3-2 [1] have been developed to limit the harmonic input current magnitudes of many ubiquitous electronic devices. These devices include: servers, desktop computers, computer monitors and modern flat-screen televisions with maximum rated input power above 75W.

In addition to harmonic input current magnitude standards, many government and industry sponsored organizations have developed certification programs specifying minimum power factor requirements for numerous household and commercial electronic goods [2–4]. Power factor is a metric describing the qualities of a load in a ac power system. Loads with a high power factor appear largely resistive to the ac mains as the line current is in-phase and proportional to the line voltage. Systems with a low power factor have phase-displaced line voltage and current, non-proportionality between line voltage and line current resulting from high harmonic current content of the line current, or both phase displacement and high harmonic current content combined.

Uncontrolled rectifiers, either half-wave or full-wave, followed by a large energy storage capacitor were traditionally utilized to perform the necessary ac rectification and supplied a close to dc output to a downstream DC-DC converter or linear regulator. The power factor of such rectifiers was low due to the peak charging of the capacitor near the peak of the ac line. Placing a controllable switched-mode converter between the rectifying elements and the large energy storage capacitor of the uncontrolled rectifier results in the configuration of a PFC rectifier.

The increasing demands by government standards and certification programs, such as the minimum power factor requirements at 50% load for AC-DC computer power supplies [2], all but eliminate the possibility of meeting such standards with a passive PFC rectifier for most designs. Therefore, active PFC controllers will see increased use in SMPS for electronic goods. While many commercial power factor controller integrated circuits (ICs) are currently available, the stricter standards and certification program requirements as well as the ever present downward pressure on implemented controller cost motivate research in this area. Furthermore, digital control techniques for controlling SMPS have been developed for many applications but few designs have enjoyed widespread market use and success. The relatively low dynamic requirements of a power factor correction controller along with the increasing use of power factor corrected SMPS provides a promising outlook for the appropriate application of digital control techniques for PFC rectifiers.

The benefits of a digital controller implementation include reduced performance variation due to age, temperature and other environmental factors, the ability to easily implement adaptive control structures and possibly a reduction in controller cost and die/package size when compared to an analog controller implementation. Also a digital controller designed for and implemented using a flexible digital platform, such as a microprocessor, complex programmable logic device (CPLD) or field programmable gate array (FPGA), enables the inclusion of other valuable control features or auxiliary functions previously developed.

This dissertation introduces a digital PFC controller for single-phase boost PFC rectifiers. This simple digital control technique, called digital non-linear carrier (DNLC) PFC control achieves excellent low harmonic input current shaping over a wide load range and over the entire universal

input voltage range (85-265V$_{rms}$). The described DNLC PFC controller is suitable for implementation in either an ASIC or in a flexible digital platform. The controller interface to the PFC rectifier stage is simplified requiring only inductor current sense, output voltage sense and gate drive output connections. The DNLC PFC controller has been implemented in an FPGA and experimental results are presented for a 300W boost PFC rectifier.

Chapter 2 of this dissertation provides a review of harmonic current and power factor standards related to single-phase PFC rectifiers followed by a brief background of common analog and digital control techniques. The DNLC PFC control is derived and analyzed in Chapter 3. Limit cycling and quantization issues of the outer voltage loop in digital PFC controllers are presented in Chapter 4. Conditions to avoid limit cycling of the power command signal are presented and examples are given for digital PFC controllers operating as either a DNLC PFC controlled or a digital average current mode (DACM) PFC controlled rectifier. Furthermore, it is shown that the DNLC PFC controlled rectifier exhibits unique properties allowing the avoidance of power command limit cycling even when the rectifier is followed by a high-efficiency regulating DC-DC converter as is commonly used in electronic power supplies. Chapter 5 introduces specialized analog to digital (A/D) converter appropriate for sensing the output voltage of a single-phase PFC rectifier. Implementation of this A/D requires only a single comparator with an analog reference voltage and a small amount of digital hardware. Analysis of the A/D structure shows that the gain of the A/D is dependent on the operating power of the PFC rectifier. Additionally, it is shown that when the SCA/D is paired with a DNLC PFC current controller the outer voltage loop bandwidth variation due to PFC rectifier power processing level is reduced. This enables outer voltage loop designs that provide improved transient performance over a broad load range. Spurred by industry, Chapter 6 presents an investigation of measuring the input power of a PFC rectifier using only digital data converted for PFC control purposes. Three different input power measurement techniques are developed and reported. A summary of the contributions and conclusions of this work, as well as possible applications and directions for future research, are presented in Chapter 7.

Chapter 2

Background

Unprecedented global growth in electronics usage has significantly changed the electrical grid's load profile in recent years. For instance, 0.8% of the entire world's electrical power was consumed by servers (primarily in commercial data centers) in 2005 and power usage was expected to nearly double by 2007 [5]. While the majority of electrical power is still consumed by traditional loads such as electric motors, resistive heating elements and traditional lighting devices, the amount of power consumed by electronic devices has become large enough to raise concerns about how the electrical grid is affected by such loads. This chapter first reviews power factor correction as it relates to switched-mode power supplies (SMPS) for powering electronic devices. Harmonic current standards and power factor certification programs are also introduced. A short review of the operation of switched-mode power converters is given as an introduction to the boost power factor correction (PFC) rectifier. Current control techniques for PFC rectifiers are then discussed. State of the art digital control techniques for PFC rectifiers are also discussed following a short introduction to the benefits of digital control.

2.1 Power Factor Correction and Applicable Standards

This section provides a perspective of different types of power factor correction and introduces the standards that apply to single-phase PFC rectifiers that are used in consumer electronics.

2.1.1 Power Factor Correction and Harmonic Currents

In alternating current (ac) power systems the term "power factor correction" has traditionally referred to the addition of reactive elements to a linear electrical load in order to align the sinusoidal voltage and current supplied to the load in phase. The power factor (PF) for pure ac systems with linear loads is [6]

$$PF = \cos\theta_{vi} \tag{2.1}$$

where θ_{vi} is the phase angle between the voltage and the current waveforms. The typical application of this type of power factor correction is adding capacitors in parallel with ac electric motors, which tend to have large inductive impedance components and draw a lagging current without power factor correction. The capacitors by themselves would draw a leading current so with the capacitors and the motor in parallel the overall system draws current in phase with the voltage leading to a near unity power factor if the capacitors are sized appropriately.

There are two main reasons why power factor correction is desirable. The first is the reduction of reactive and real power necessary to supply the load. When an ac connected load has a power factor not equal to unity the load is seen as either a reactive power source or sink. This power is not actually generated or consumed by the load but rather is stored by the load and then released back to the ac mains during every ac line cycle. This results in additional current in the ac mains compared to the current required to supply the load if the load had a power factor of unity. These additional currents cause increased resistive losses in the transmission and distribution system feeding a load even though they don't supply any real power to the load. Reactive currents also effectively reduce the amount of real power a transmission and distribution system, which are current capacity limited, can deliver to a load. Appropriately, electrical transmission and distribution companies advocate for ac load PF requirements or specifications which allow the transmission and distribution lines to carry more marketable power without the need for capital intensive line upgrades. The second reason is to reduce harmonic pollution and transformer losses within the distribution system. Non-linear loads connected to the ac mains, as described below, can draw line current with high harmonic

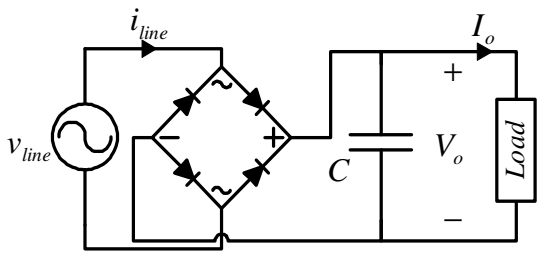
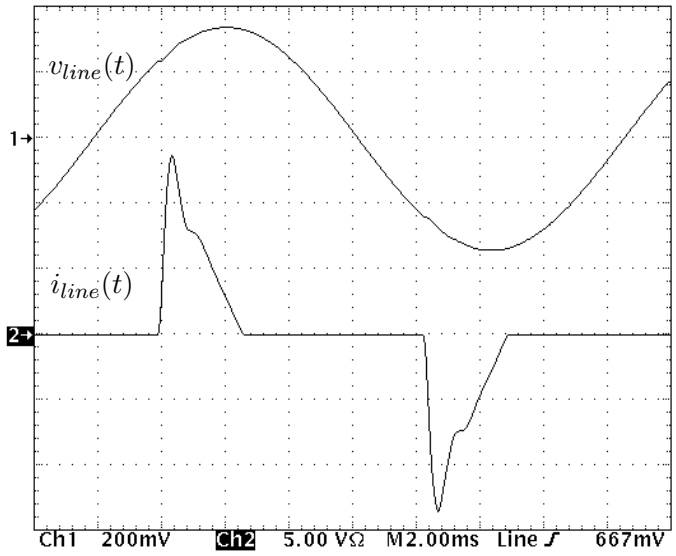


Figure 2.1: Uncontrolled full bridge rectifier with a large output capacitor.

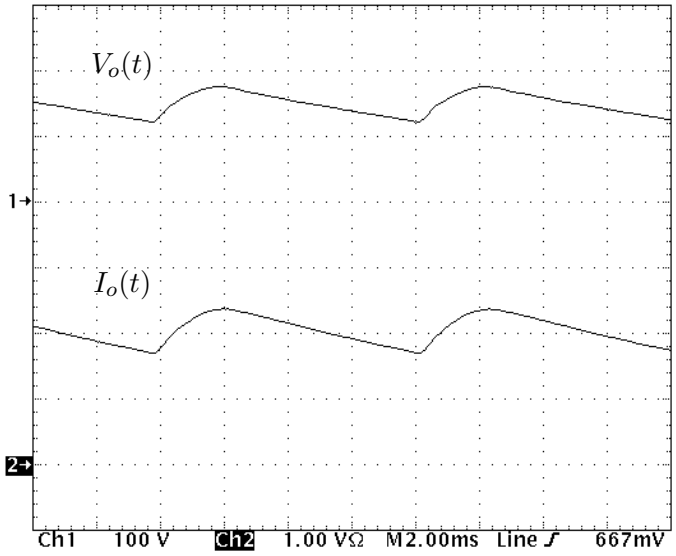
current content. These harmonic currents can pollute the local ac distribution system causing ac equipment malfunction, distorted ac line voltage and system reliability issues. Furthermore, harmonic current content leads to increased local distribution transformer losses due to operation of power system transformers at line harmonic frequencies for which they were not designed to operate.

Power factor correction for electronic power supplies, as are found in electronic devices such as televisions, computers, computer monitors and servers, is considerably different than power factor correction for ac power systems. A typical power supply for electronic devices takes ac power from the ac mains and supplies direct current (dc) power to device circuitry. The need for rectification, converting ac power to dc power, in electronic device power supplies precludes traditional power systems based power factor correction techniques.

In order to understand why power factor correction is beneficial to the overall power system it is helpful to examine how non-power factor corrected rectifiers operate. Fig. 2.1 shows a simple full-bridge rectifier circuit used generate a near dc output voltage given an ac input. Current flows from the ac line only when the instantaneous input voltage is larger than the instantaneous capacitor voltage. The load seen by the ac line is non-linear as it has a finite impedance only when current is flowing from the input to the output and infinite impedance otherwise. Fig. 2.2(a) shows the line voltage ($v_{line}(t)$) and the line current waveforms ($i_{line}(t)$) for the operation of the circuit shown in Fig. 2.1 with $V_{line,rms} = 120$V, $C = 220\mu$F. The average power processed by the full-bridge rectifier is 300W. The line current waveform clearly shows large periodic peaks containing many current



(a) Uncontrolled full bridge rectifier inputs.



(b) Uncontrolled full bridge rectifier outputs.

Figure 2.2: Uncontrolled full bridge rectifier input and output waveforms.

harmonics. Fig. 2.2(b) shows the output voltage and current waveforms under the same operating parameters mentioned above. The output voltage, V_o, is not constant but does have a significant dc component that is supported by the discharging of the capacitor during periods when the output voltage is higher that the input voltage.

A different definition of PF is needed to describe the periodic non-sinusoidal waveforms of the line current caused by the non-linear ac load shown in Fig. 2.2(a). By describing the input current waveform in terms of it's Fourier series components a complete expression of the power factor can be found as [7],

$$PF = \left(\frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} \right) \cos\theta_{vi} \tag{2.2}$$

$$= (\text{distortion factor})(\text{displacement factor})$$

where (I_2, I_3, etc.) are the magnitude of the Fourier series components of the line current at 2×, 3×, etc. of the fundamental line frequency (f_{line}). This definition of power factor shows that the magnitudes of the harmonic currents effect the power factor as does the phase difference between the supplied voltage and current. Additionally, as shown in (2.2), the PF has two components. The first component is the distortion factor (sometimes denoted by DF) which relates the ratio of the rms fundamental component to the rms of all the frequency components of the waveform. The second factor, called the displacement factor, matches the original PF equation (2.1) for linear ac systems.

The ratio of the rms value of the harmonic components of a waveform and the rms value of the fundamental waveform components is defined as the Total Harmonic Distortion (THD) [7],

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1}. \tag{2.3}$$

The THD of a given waveform gives a rough measure of the waveforms harmonic content in the form of a convenient single number. However, the THD does not indicate which harmonic current

or currents, $3^{\text{rd}}, 4^{\text{th}}, ..., n^{\text{th}}$, are contributing to the harmonic distortion. The THD is also a more sensitive measurement than DF for the rough estimation of the harmonic content of current waveforms in many instruments with fixed precision readout. For instance, a DF of 0.9 (or PF of 0.9 assuming a displacement factor of unity) corresponds to a THD of 48.4%.

2.1.2 Harmonic Current Limits and Power Factor Standards

As shown in (2.2), the power factor is a function of the magnitudes of the harmonic currents of the line current. Reducing the magnitudes of harmonic currents above the fundamental inherently improves the systems power factor. Standards limiting the amount of harmonic current allowed have developed in two forms. Some standards have been developed that directly limit the magnitude of the harmonic current for each harmonic order. Others specify a power factor that must be obtained under certain line and load conditions, effectively limiting the maximum amount of harmonic current permissible assuming that the input voltage and current are in phase.

2.1.2.1 EN 61000-3-2

The International Electrotechnical Commission (IEC) published a standard limiting line harmonic distortion caused by electrical and electronic equipment with an input current up to 16A per phase (IEC 1000-3-2) in 1995 [8]. The same year the European Committee for Electrotechnical Standardization (CENELEC) adopted the IEC's recommendation by publishing EN 61000-3-2.

The EN 61000-3-2 standard outlines four classes of equipment used to determine the amount of harmonic current distortion allowed. Class A equipment is all equipment not considered to be any other class. Class B equipment includes portable and arc welding equipment. Class C equipment includes all lighting equipment and Class D equipment specifically includes personal computers, monitors and televisions with a input power of less than 600W [1]. Harmonic currents are measured at a nominal line voltage of 230V with the PFC rectifier operating at full rated power. Class A harmonic limits are given as absolute limits with the units of amps (A), whereas Class D harmonic limits are normalized by the rated power of the PFC rectifier resulting in harmonic limits

with the units of milliamps per watt (mA/W).

The more stringent Class D harmonic limits are used as a current harmonic metric throughout this thesis as the target application is for power factor correction of computer and server power supplies.

While the EN 61000-3-2 standard is technically only applicable to equipment sold in Europe and surrounding CENELEC affiliates the standard has become more generally adopted because of many major electronics manufactures desire to market universal products; products fit for sale anywhere in the world. Requirements for a universal input product are challenging. For instance, a product must operate properly over a input voltage range of $85 - 265V_{rms}$ in order to be universal input voltage compliant. Line frequencies of both 50 and 60Hz must also be considered in the product design. Due to the desire for universally marketable products the EN 61000-3-2 standard must be met for a large quantity of electronics regardless of their final point of sale. Also, in the U.S. which does not have a harmonic current standard, many EN 61000-3-2 compliant products are sold as premium products and claim increased performance over similar products without power factor correction.

2.1.2.2 JIS C 61000-3-2

The Japanese Industrial Standards (JIS) Committee has adopted a modified version of the EN 61000-3-2 for regulation of current harmonic pollution in Japan. These harmonic current limits are equivalent to the EN 61000-3-2 limits except they have been scaled by the ratio of the nominal line voltage in Europe and the nominal line voltage in Japan (230V/100V = 2.3). This scaling normalizes the harmonic current limits so that the power present in the line harmonics are equivalent regardless of which line voltage is considered. The adoption of this standard also suggests that a North American harmonic current standard, if adopted, would likely be equivalent to the EN 61000-3-2 standard multiplied by 230V/120V = 1.92. Throughout this thesis Class D limits for nominal line voltages other that 230V have been scaled accordingly.

2.1.2.3 Certification Programs: Energy Star® and 80 Plus®

Various product certification programs, also known as labeling programs, have been developed to encourage the general use of power supplies with improved efficiency and input power factor. The Energy Star® program, a joint venture of the U.S. Environmental Protection Agency and the U.S. Department of Energy, provides certification of a variety of commercial and household electrical appliances and devices. Specifically, Energy Star® certification standards for computers [3] and servers [4] are of interest to this work. Additionally, an industry sponsored organization, 80 Plus®, has also developed a certification program. This program currently features a total of eight certification levels: four regarding 115V computer applications and four regarding 230V server applications.

Table 2.1: Minimum PF requirements for popular certification programs.

Line Voltage	Min. PF at Percent Load		
(V_{rms})	20%	50%	100%
Energy Star® for Servers v.1			
115/230†	0.8	0.9	0.95
Energy Star® for Computers v.5			
115/230	-	-	0.9
80 Plus® Platinum			
230‡	-	0.95	-
80 Plus® Gold			
115/230‡	-	0.9	-
80 Plus® Silver			
115/230‡	-	0.9	-
80 Plus® Bronze			
115/230‡	-	0.9	-
80 Plus®			
115‡	-	-	0.9

† For AC-DC Multi-output

‡ 115V specifications are for computers only, 230V specifications are for servers only.

Table 2.1 shows the minimum PF requirements for the different certification programs. The most comprehensive PF specification is Energy Star® for servers v.1 which requires a minimum PF of 0.95 at full load and a minimum PF of 0.8 at 20% load. Certification for 80 Plus® requires

a power factor of 0.9 at 50% load for all certification levels except for the dated 80 Plus® level, valid only for 115V computer power supplies, and the 80 Plus® Platinum level which is available only for 230V servers specifically designed for use in data centers.

2.2 Boost Converter Fundamentals

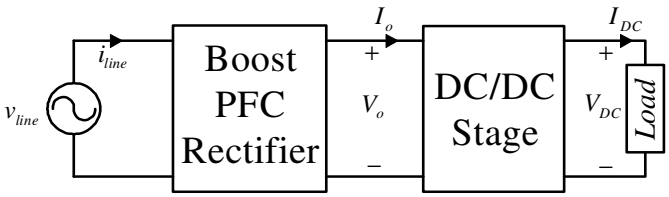


Figure 2.3: Typical power supply block diagram.

PFC rectifiers are typically only part of a electronics power supply. A typical complete power supply, shown in Fig. 2.3, uses a boost PFC stage which processes the ac input power into a loosely regulated dc output voltage (V_o) that is often in the 380-400V range. A DC-DC switched-mode power supply is then often used to process the power available at the output of the boost PFC stage up or down in voltage to well regulated dc outputs required by a specific application. The boost converter topology has the least switch stress and lowest parts count of any suitable PFC converter topology and thus it is the most prevalent PFC stage. The steady state dc characteristics of the boost converter are provided here as a necessary introduction for the derivation of the digital non-linear carrier (DNLC) PFC controller presented in Chapter 3.

The objective of a boost converter, shown in Fig. 2.4, is to provide a relatively constant output voltage (V_o) that is larger than the input voltage (V_g). Simple inspection of Fig. 2.4 reveals that the output voltage cannot be less than the input voltage (assuming no losses in the stage) because there is a direct connection between the input and output via the inductor and diode. The converter switches at a switching frequency of f_s ($T_s = 1/f_s$) and the percentage of the time that switch Q_1 is on during T_s is denoted as dT_s where d is called the duty cycle for switch Q_1. Characteristic steady state waveforms for the boost converter are shown in Fig. 2.5.

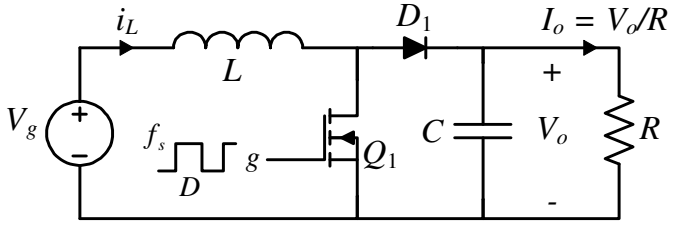


Figure 2.4: DC-DC boost converter.

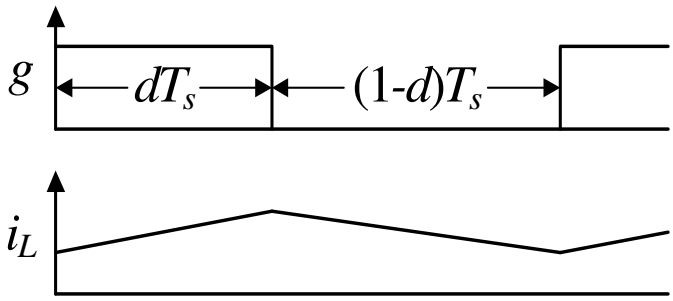


Figure 2.5: DC-DC boost converter characteristic waveforms.

During the interval dT_s, Q_1 is on and the voltage across the inductor is V_g. Also, the load current (I_o) is supplied entirely from the output capacitor during this interval. The following two equations represent the inductor and capacitor dynamics during $t < dT_s$.

$$L\frac{di_L}{dt} = V_g \tag{2.4}$$

$$C\frac{dv_o}{dt} = -\frac{v_o}{R} \tag{2.5}$$

Similarly, during the interval $T_s > t > dT_s$ the voltage across the inductor is $V_g - v_o$ and the capacitor current is $i_L - v_o/R$. The inductor and capacitor dynamics during this interval, denoted as $(1-d)T_s$, are:

$$L\frac{di_L}{dt} = V_g - v_o \tag{2.6}$$

$$C\frac{dv_o}{dt} = i_L - \frac{v_o}{R} \tag{2.7}$$

To capture the low frequency behavior of the boost inductor (2.4) and (2.6) can be combined as:

$$L\frac{di_L}{dt} = dV_g + (1-d)(V_g - v_o) = V_g - (1-d)v_o \tag{2.8}$$

(2.5) and (2.7) are also combined giving the low frequency behavior of the output capacitor.

$$C\frac{dv_o}{dt} = -d\left(\frac{v_o}{R}\right) + (1-d)\left(i_L - \frac{v_o}{R}\right) = (1-d)i_L - \frac{v_o}{R} \tag{2.9}$$

Assuming that the ripple magnitude in v_o and i_L is small and that $d = D$, meaning the duty cycle ratio is constant, these values can be approximated as steady dc values of V_o and I_L respectively. Also, in steady state operation the capacitor voltage and inductor current should be constant when averaged over T_s. This results in the derivatives of (2.8) and (2.9) being zero and the equations simplify giving the dc voltage conversion ratio,

$$\frac{V_o}{V_g} = \frac{1}{1-D} \tag{2.10}$$

and the relation for the dc inductor current,

$$I_L = \frac{V_o}{R(1-D)} = \frac{I_o}{1-D}. \tag{2.11}$$

2.3 Boost Converter as a PFC Rectifier

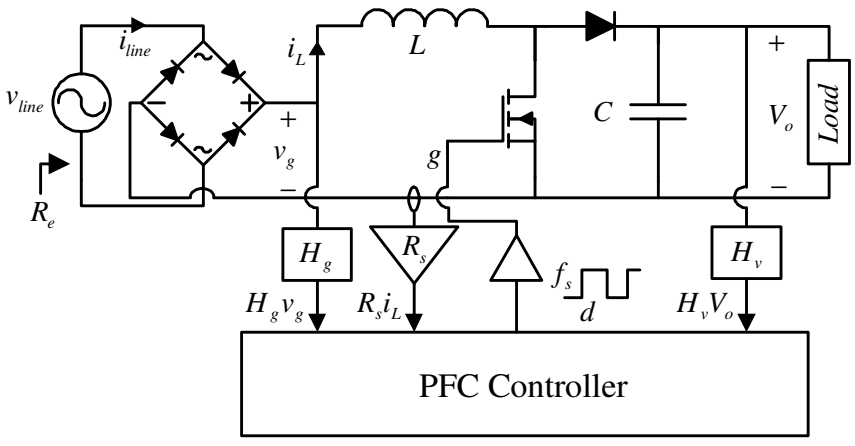


Figure 2.6: Basic schematic of a boost PFC rectifier.

A basic schematic of a boost PFC rectifier is shown in Fig.2.6. A full bridge rectifier has been added to the input of the boost converter shown in Fig. 2.4. This rectifies the ac mains so that the

input seen by the boost converter is always positive. A PFC controller block is also shown that processes inputs from the boost stage and generates a gate drive signal. The controllers objective is to adjust the gate drive so that the inductor current, which is also the unrectified input current, is shaped in such a way that harmonic distortion is minimized. Inspection of (2.10) shows that V_o must be higher than v_g to maintain realizable positive duty cycle ratios. Universal input PFC designs usually accommodate rms line voltages up to 265V. This results in a maximum peak input voltage of about 375V. For these types of designs V_o must be greater than 375V. The range of typical regulated PFC output voltage is from 380-400V.

2.4 Boost PFC Rectifiers with Analog Control

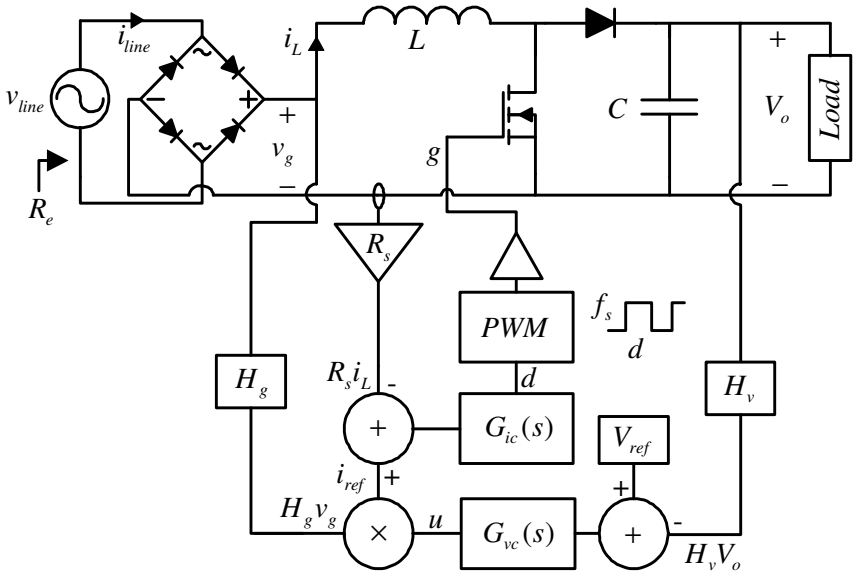


Figure 2.7: Analog average current mode PFC block diagram.

Many analog control solutions have been developed for PFC rectifiers. One of the most prevalent analog solutions is average current mode (ACM). Fig. 2.7 shows a simplified block diagram of a single-phase ACM PFC [9–11]. Operation of the ACM PFC rectifier is straightforward. In order to obtain low harmonic distortion of the input current (i_{line}) the desired emulated input resistance

(R_e) at the PFC input should be constant during a line cycle. In order to obtain a constant R_e the input current must be in phase and proportional to the line voltage. In ACM PFC control an inner current loop with compensator $G_{ic}(s)$ is used to regulate the average inductor current at a reference current (i_{ref}). An analog multiplier is utilized to create an i_{ref} that is proportional to the rectified input voltage (v_g) and a power command signal u. The power command signal u is adjusted by an outer voltage loop with compensator $G_{vc}(s)$ that adjusts the value of u in order to regulate the output voltage of the PFC.

The inner current loop needs to be able to track the reference current with a relatively high bandwidth in order to reduce input current distortion during zero crossings. Conversely, the outer voltage loop requires a low bandwidth in order to avoid distortion in the input current waveform. This is due to the existence of a considerable voltage ripple on the output at $2f_{line}$. This ripple is due to the inherent instantaneous power imbalance between the ac input and dc output of the PFC rectifier. During zero-crossings of the input voltage and current the power supplied to the PFC stage is zero regardless of controller action. As the output is supplying a constant or near constant load in normal operation the output voltage drops when the power processing of the PFC stage is lower than the output power draw. Likewise, the output capacitor is charged and the output voltage increases when the instantaneous input power is greater than the output power draw. The resulting low frequency ripple on the output occurs at $2f_{line}$ since there are two zero crossings of the input voltage and current during each line cycle. In practical ACM PFC circuits with a line frequency of 50-60Hz the inner current loop bandwidths are often between 2-10kHz, with the realizable bandwidth being a function of the chosen switching frequency. The upper limit for the outer voltage loop bandwidth is about 40Hz although maximum voltage loop bandwidths below 10Hz are also implemented in some designs.

As the name implies, the current control loop tracks the average input current over a switching period ($\langle i_g \rangle_{T_s}$). Low pass filtering of the instantaneous input current by either a separate current sense amplifier or by the dynamic filtering of $G_{ic}(s)$ generates control actions that are based on the average input current. This allows the ACM PFC to operate in either continuous conduction mode

(CCM) or discontinuous conduction mode (DCM), a mode where both the boost switch and the diode do not conduct during a portion of the switching period, with low harmonic current shaping.

For ACM PFC control three sensed converter values are needed for operation. The rectified line voltage (v_g) is needed as a template for input current waveshape. The inductor current (i_g) is required to close the inner current loop so that the reference current can be tracked. Additionally, the PFC rectifier output (V_o) needs to be sensed to close the outer voltage loop and regulate the output voltage at a desired level.

In addition to ACM, one-cycle control [12, 13] and nonlinear-carrier control [14] are analog control solutions used for PFC rectifiers. One-cycle control and nonlinear-carrier control require only an input current sense and an output voltage sense, simplifying PFC rectifier design and implementation. Both control strategies also provide the option of sensing the transistor switch current instead of the inductor current as the average inductor current is not needed for control as in ACM PFC control.

2.5 Digital Control of Switched-mode Power Converters

Digital control, juxtaposed to analog control of switched-mode power converters, presents many possible advantages and challenges. To implement digital control all necessary data inputs must be digitized using an analog-to-digital converter (A/D). The digital outputs of the digital controller must also be interfaced to the system being controlled, often by a digital-to-analog (D/A) converter. In the case of switched-mode power converters, a digital pulse width modulator (DPWM) often replaces the digital controller output D/A and analog PWM. This eliminates the need for a traditional D/A but requires that the digital controller be able to produce a modulated duty cycle with a reasonable temporal resolution.

The functionality of a digital controller can be described by digital control laws that are written as difference equations. Depending on the input to the digital controller, different control laws may be implemented allowing an adaptive change in control.

The hardware that constitutes a digital controller can be realized in a number of ways.

The first is an application specific integrated circuit (ASIC) where the digital functionality of a designed digital controller is implemented directly in silicon. A digital controller can also be implemented in a programmable logic device such as an field programmable logic array (FPGA). The functionality of the digital controller is coded using a hardware descriptive language (HDL) such as Verilog or VHLD. This code is then compiled and the FPGA is programmed to realize the digital controller in hardware. Microprocessors are also commonly used to implement digital controllers. The microprocessor is programmed so that the control laws of the desired digital controller are computed. Implementation of a digital controller in either a programmable logic device or a microprocessor allows for the option of modifying the digital controller functionality after initial placement in to a system (field programmability).

Digital controllers do suffer from latency issues not present in analog control implementations. The first latency issue involves the sample rate of the A/Ds used to sense controller inputs. These A/Ds typically convert at a fixed rate that directly affects the response of the controller to a disturbance. If a disturbance occurs right after the previous sample point, the digital controller will not respond to the disturbance until the next sample instance. Additionally, the time it takes to process the digital inputs and generate a proper control output requires a finite amount of time depending on the type of hardware used to implement the controller and the controller clock rate. For ASIC and FPGA implementations processing of the appropriate control output can be computed in parallel requiring a minimum of one clock cycle after the controller inputs are valid. Microprocessor implementations often take far longer or require a high performance microprocessor to compute the control law as common microprocessors compute serially, thus requiring a number of clock cycles to produce an output.

The control of PFC rectifiers is often considered to be one of the first power electronics applications where digital control is expected to supercede analog control. This is primarily due to the low dynamic performance needed to shape the rectifier input current and the specific advantages digital control presents. The following advantages of digital control have motivated this research in digital control of PFC rectifiers:

- **Ease of controller implementation and reduction of discrete components**

  As digital controllers are implemented using equations instead of analog electronics, specific digital compensator parameters can be easily adjusted either internally or externally from the controller. This eliminates the need for discrete components required for compensation circuits in analog compensators. Additionally, some digital control laws do not require any adjustment between various power converter designs decreasing the required design effort for a new product.

- **Adaptive control**

  Adaptive control refers to changing the implemented control law depending on present or past controller inputs. While it is not impossible to implement adaptive control with an analog controller it is considerably simpler to accomplish with digital controllers. Also, the incremental cost of including adaptive control is relatively low once a digital controller is implemented. Adaptive control is attractive due to it's use particularly in realizing higher bandwidth regulation and converter efficiency improvements due to adaptive control actions.

- **Reduced sensitivity to parameter tolerances**

  The impedance of discrete components change with temperature and with the increasing age of the component. When used in analog controllers, specifically for control loop compensation, the resulting compensator can change significantly over time or with a considerable temperature change. As a digital controller's control law is not implemented with discrete components these effects due to temperature and aging are completely avoided.

- **Controller cost**

  With the ever increasing density of digital logic prevalent in the computer processor industry, it is conceivable that a digital controller might eventually become more inexpensive than available analog controllers. This is particularly true for full-featured digital con-

trollers as adding features in digital design does not greatly increase the cost of a controller whereas additional features in analog controllers often greatly increases their cost.

The following sections provide an overview of state of the art digital control strategies for single-phase PFC rectifiers based on the boost converter. While there are many control strategies for lower power operation, such as constant duty cycle control in DCM and various critical conduction mode control methods, control strategies that operate primarily in CCM during full load operation are reviewed here. These digital control topologies are more commonly used for medium to high power PFCs (nominal output power between 200W-2kW) when high converter efficiency is desired. Section 2.5.1 discusses the commonly implemented digital average current mode controller. A similar controller with improved current shaping potential, the predictive current mode controller, is described in Section 2.5.2. A digital inductor charge controller is briefly discussed in Section 2.5.3 to illustrate the difference between digital control strategies that emulate analog control methods and digital control strategies that take advantage of discrete control properties. Lastly, Section 2.5.4 discusses hybrid PFC controllers which offer a mix of the characteristics of their analog and digital controller derivatives.

2.5.1 Digital Average Current Mode PFC Rectifiers

A block diagram of a digital average current mode (DACM) PFC rectifier is shown in Fig. 2.8. Comparison of this figure with Fig. 2.7 quickly reveals the similarities of the analog and digital versions of average current mode control. Both utilize a fairly high bandwidth inner current loop and a slower outer voltage loop that determines the power processing level of the PFC stage. In DACM control the rectified input voltage (v_g), inductor current (i_g), and output voltage (V) are digitized and the analog compensators are replaced by digital compensators ($G_{ic}(z)$ and $G_{vc}(z)$). The output of the digital current loop compensator feeds a DPWM which generates a discrete time gate driving waveform (g).

The average inductor current during a switching period ($\langle i_g \rangle_{T_s}$) is determined by sampling

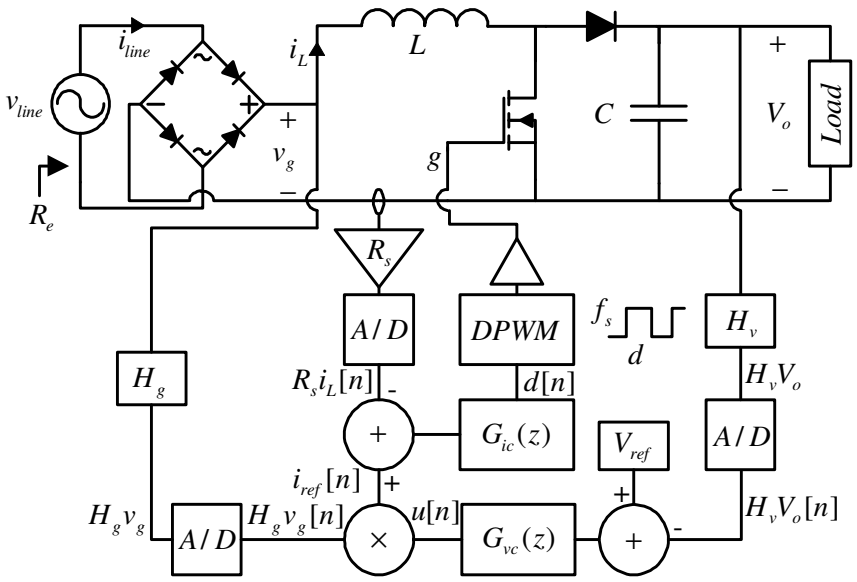


Figure 2.8: Digital average current mode PFC boost rectifier.

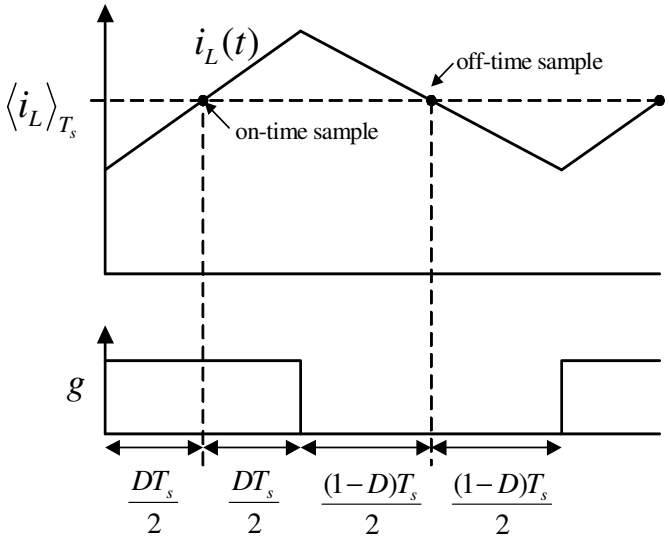


Figure 2.9: Digital sampling of the average inductor current.

the inductor current either during the middle of the gate conduction time (on-time) or the middle of the diode conduction time (off-time). Fig. 2.9 shows how the single point sampling results in the average value of the inductor current. Timing signals to sample during the on or off-time

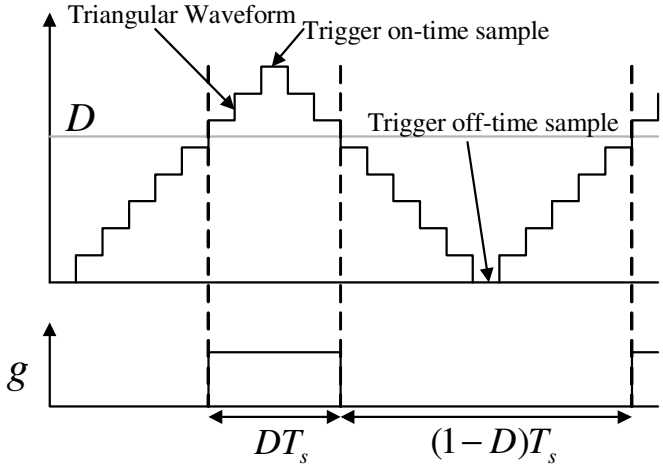


Figure 2.10: Sampling during the on or off-time using a triangular DPWM.

are easily generated in the digital controller using a triangular DPWM. In contrast to a typical ramp type DPWM the triangular DPWM modulates both the rising edge and falling edge of the pulse width. Fig. 2.10 shows characteristic internal waveforms of the triangular DPWM. On-time inductor current samples are triggered when the triangular ramp reaches it's maximum possible value. Off-time inductor current samples are collected by triggering the A/D at the bottom of the triangular carrier.

Implementations of DACM PFC control have been reported by [15–19]. Some of the reported work on DACM PFC has related directly to the quality of input current waveshaping while others have reported added features or performance improvements in outer voltage loop transient responses. A DCM sample correction method was reported by [19] and was meant to increase the quality of input current waveshaping around the zero-crossings of the input voltage particularly at light load. When using timed samples of the inductor current to determine the average inductor current, operation in DCM will result in incorrect average current values. Correction factors can be used to compensate for the erroneous sampled inductor current when the digital controller determines that the PFC will operate in DCM during a particular switching period.

A method for estimating the rectified line voltage when the switch node voltage is sensed,

thus eliminating the need to sense v_g, is proposed in [18]. This method allows for a high level of integration and a low pin count implementation as the required sensed switch node voltage would be internally connected on a chip with an integrated boost switch.

There has also been considerable interest in increasing the outer voltage loop's bandwidth during load or line transients. While a higher bandwidth voltage loop transient response distorts the input current waveshape, the PFC output voltage could be regulated inside a much tighter range possibly allowing cost savings in the downstream DC-DC converter. Two distinct methods have been proposed that allow for effective low bandwidth operation in steady state and quickly responding corrective actions during transients. First, a method involving filtering of the output voltage waveform is discussed. Secondly, a method that takes advantage of the quantization effects present in the sensing of the output voltage is presented.

Filtering of the sensed PFC output voltage with the aim of removing frequency content at $2f_{line}$ is proposed in [15] and [16]. A notch filter, positioned at a frequency of $2f_{line}$ is proposed by [15] and shows that with the output voltage ripple sufficiently attenuated the dynamic response of the outer voltage loop is improved compared to the case with no output voltage filtering. This dynamic improvement, although small, is achieved with an outer voltage bandwidth of 20 Hz. One drawback of this proposed controller is that the notch filter is fixed in frequency and does not adapt according to which line frequency the PFC input is connected. This make this controllers implementation difficult in universal product designs as both 50Hz and 60Hz line frequencies are common around the world. An adaptive filter that tunes itself to the line frequency is proposed in [16]. In addition to attenuating the output voltage ripple using a digital comb filter, this study implements a higher bandwidth outer voltage loop for increased dynamic performance. The bandwidth of the outer voltage loop is reported to be higher than $2f_{line}$ but does not cause input current distortion in steady state and the dynamic performance is improved significantly during transients.

A method that uses the quantized nature of the output voltage sense to detect when a transient is occurring is reported in [17]. Referring to Fig. 2.11, a dead-zone is established consisting of one or more quantization bins of the output voltage sense. The ac coupled output voltage is

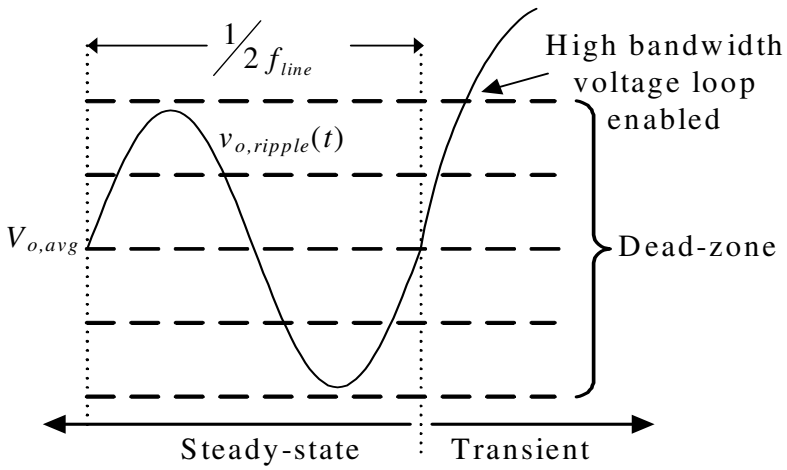


Figure 2.11: Pictorial diagram of dead-zone implementation and transient detection.

shown and horizontal lines denote quantization bins of the output voltage sensing A/D around the regulated output voltage. If the sensed voltage samples are inside the dead-zone a slow voltage loop is implemented. However, output voltage samples sensed outside of the dead-zone trigger a different mode of operation for the digital voltage loop compensator. Typically the digital voltage loop compensator coefficients are modified in this "fast voltage loop" mode to create a higher bandwidth control loop. Once the output voltage samples return to the dead-zone the slow voltage loop is again implemented for normal operation. During steady state operation the entire sensed voltage waveform must be contained in the dead-zone. As the output voltage ripple magnitude varies with the power processing level of the PFC stage and the capacitance seen at the output a method to adaptively adjust the size of the dead-zone is also proposed in [17]. The dead-zone approach is easily implemented since the output voltage must be digitized which automatically results in the quantization levels utilized in dead-zone control. It is however necessary to have a relatively high resolution output voltage A/D in order to keep the dead-zone from being too large which may increase the cost of the digital implementation.

2.5.2 Predictive Control

Predictive control, where the next control value is computed using current measured system values and system behavioral equations, is ideally suited to digital implementation. Assuming a boost converter operates in CCM the behavioral equations can be represented as the inductor current dynamics.

Digital predictive control for PFC rectifiers is reported in [20] and [21]. Both reported implementations use a DSP to realize the digital controller. In [20] the next duty cycle necessary to track a PFC reference current is calculated using sampled values of the input and output voltage as well as the difference between the sampled inductor current and the reference current. The value of the boost inductance (L) is also required to complete the next duty cycle calculation. The calculations providing the predicted solutions are relatively complex and are computed during every switching period as in [20]. However, the entire switching period can be used to calculate the next duty cycle command. In short, predictive control requires somewhat burdensome calculations but the solutions are not required immediately for control. This makes predictive control of PFC's attractive when a DSP or microprocessor is available for control purposes.

In [21] a predictive control method is proposed that does not require the sensing of the inductor or switch current. A sine wave look up table scaled by the voltage loop derived power command signal is utilized to generate the current reference. The next duty cycle command is then calculated according to a predictive equation. This predictive PFC control topology effectively operates with no error feedback for current control. Satisfactory results appear possible as long as converter variables such as input voltage, output voltage and boost inductance values are accurately known.

By its nature predictive control requires many system value to be sensed or at least estimated. The aggregate accuracy of these sensed values directly effects the quality of the resulting control. Predictive control is also not ideally suited for implementation as a general control chip as the boost inductor value is required for control. The inductance value could be communicated to the

control chip via a serial interface but this would require more controller pins, increasing controller cost and design complexity.

2.5.3 Inductor Charge Control

An implementation of digital inductor charge control for PFC rectifiers has been reported in [22]. In this control scheme the inductor current is sampled multiple times during a switching period. These collected samples, starting when the converter's switch (a PFC flyback converter in this study) is turned on, are accumulated in a register. The accumulation effectively integrates the inductor current waveform generating an indication of the amount of charge in the boost inductor. When this accumulated value equals or exceeds a reference value whose waveshape is derived from the multiplication of the input voltage and the power command signal from the outer voltage loop compensator, as in DACM PFC control, the converter's switch is turned off.

This study shows the difficulty of implementing a digital version of a well known analog control technique. In an earlier study [23] that used analog charge control for a PFC flyback converter it was shown that such control effectively controls the average inductor current if the switching period is constant. In the analog implementation the charge controller is realized using simple hardware and results in a cost-effective method of tracking the average current. In the digital implementation multiple samples of the inductor current are required during the dT_s period. This requires a faster A/D and possibly a higher resolution A/D in order to accurately sense the ripple magnitudes than in a DACM PFC controller. Other than the possibility to also use the multiple current samples to limit peak inductor currents and the inherent noise immunity benefits to accumulating multiple current samples, there seem to be no realizable advantages to this method over other digital control techniques. The reported digital inductor charge control method in [22] is in fact simply a direct digital implementation of the analog inductor current mode controller. Inspection of the control waveforms of both the analog and digital inductor charge controllers are identical except for the discretization and quantization of the digital controller's signals. Direct digital implementations, like digital charge control above, require high speed digital implementations as

their performance is directly linked to the total latency between sample/control update instances. The analog predecessors of these digital controllers have effectively no latency so performance is limited only by parasitic effects in implementation. The cost and design burden of implementing a fast digital controller instead of a analog controller must be counteracted by the added benefits of digital control such as improved aging characteristics and the ability to implement adaptive control.

2.5.4 Hybrid PFC Control

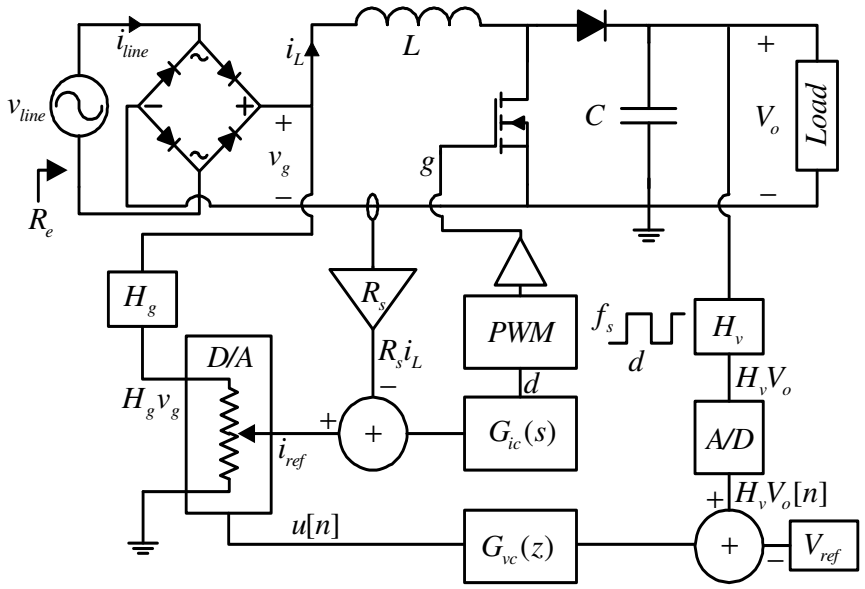


Figure 2.12: Hybrid ACM PFC boost rectifier with a digitally controlled variable resistor D/A implementation.

A control topology that uses an analog current loop and digital voltage loop is shown in Fig. 2.12. This control method is a hybrid of the ACM PFC from Section 2.4 and the DACM PFC from Section 2.5.1. Similar hybrid PFC control methods and hardware implementations have been proposed by [24–27]. This proposed controller uses a low resolution digital resistor to digitally scale the scaled rectified line voltage $H_g v_g$ to supply the analog i_{ref} waveform. The goal of implementing this topology is to provide the high bandwidth inductor current tracking performance of an analog ACM PFC controller with the advantages afforded by a digital voltage loop. Among

these advantages is an adaptive voltage loop that implements a higher bandwidth voltage loop response if the converter output voltage is far from regulation. Identical to an ACM current loop, this topology's current loop requires custom current compensation for each product designed and is susceptible to discrete component tolerances and aging issues. However, the hybrid topology does allow for the implementation of a digital voltage control loop with all the possible benefits such as: simpler and lower cost hardware implementation, reduced effects due to component aging and the ability to implement a fast voltage loop. These advantages make hybrid PFC control methods attractive. Chapter 5 presents a outer voltage loop A/D structure that extends the performance of NLC/DNLC controlled PFC stages while simplifying the digital hardware implementation. This A/D concept is particularly advantageous when paired with an analog NLC current loop.

Chapter 3

A Simple Digital Power Factor Correction Rectifier Controller

This chapter introduces a single-phase digital power factor correction (PFC) control approach that requires no input voltage sensing or explicit current loop compensation, yet results in low-harmonic operation over a universal input voltage range and loads ranging from high-power operation in continuous conduction mode down to near-zero load. The controller is based on low-resolution A/D converters and DPWM, requires no microcontroller or DSP programming, and is well suited for a simple, low-cost integrated-circuit realization, or as an hardware description langauge (HDL) core suitable for integration with other power control and power management functions. Experimental verification results are shown for a 300W boost PFC rectifier.

Single-phase power factor correction (PFC) boost rectifiers are used in a wide range of applications that are required to meet the EN 61000-3-2 standard [1]. Furthermore, certification programs, such as 80 Plus [2], specify new power factor minimums at operating powers less than full rated power. At low-to-medium power levels, transition-mode control (i.e. critical conduction mode, or operation at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM)), which offers simplicity and performance advantages, is widely used and supported by a range of commercially available low-cost controllers [28, 29]. At higher power levels (above several hundred Watts), CCM operation is often preferred because of lower conduction losses and reduced EMI filtering requirements. Averaged current mode control in combination with a slow voltage control loop and a multiplier, which is a well-known control approach for CCM PFC [11], requires a more complex implementation compared to the transition-mode control.

With the motivation of simplicity comparable to transition-mode or DCM operation, together with low-harmonic, low conduction loss, and low EMI performance in CCM, a nonlinear-carrier (NLC) control technique for CCM boost converters was introduced in [14]. In the NLC approach, the input voltage, v_g, in the PFC current control objective is expressed in terms of the output voltage, V_o, and the switch duty cycle, d, thus eliminating the need to sense the input voltage. Furthermore, [14] showed that the resulting reformulated control objective can be realized using relatively simple analog circuitry using a modulator where a periodic carrier waveform is obtained by replacing d with t/T_s in the control objective, where T_s is the switching period. As a result, this approach further eliminated the need for current loop compensation, and the need for a precision analog multiplier. In the cases considered in [14] nonlinear carrier waveforms were employed, which is why the nonlinear-carrier (NLC) term was used to name the approach. Various modifications and extensions of this approach, including implementations based on linear carrier waveforms [12,30–32], and with applications to other converters [12, 31, 33] have been reported. Furthermore, related approaches are now used in commercially available PFC controllers [34–36].

Digital PFC controllers, offering improved system interface, power management features, support for multi-module operation, and improved voltage-loop dynamic responses, have recently received increased attention. Most of the digital PFC control techniques reported so far have been based on DSP or microcontroller implementations (e.g. [9, 15, 17, 19, 21, 37–40]), or have relied on multiple current samples per switching period [22, 41].

Based on the approach presented in [14], this chapter introduces a digital PFC control approach, called the digital non-linear carrier (DNLC) PFC controller, using a simple current control law that allows operation in CCM without input voltage sensing. Further objectives are to show how low-harmonic operation over a universal input voltage range and a wide range in power can be achieved using low-resolution A/D converters, a low-resolution digital pulse-width modulator (DPWM) and minimal digital hardware. Fig. 3.1 shows a block diagram of a PFC boost rectifier with the proposed DNLC PFC controller.

This chapter is organized as follows: Section 3.1 introduces the DNLC PFC current control

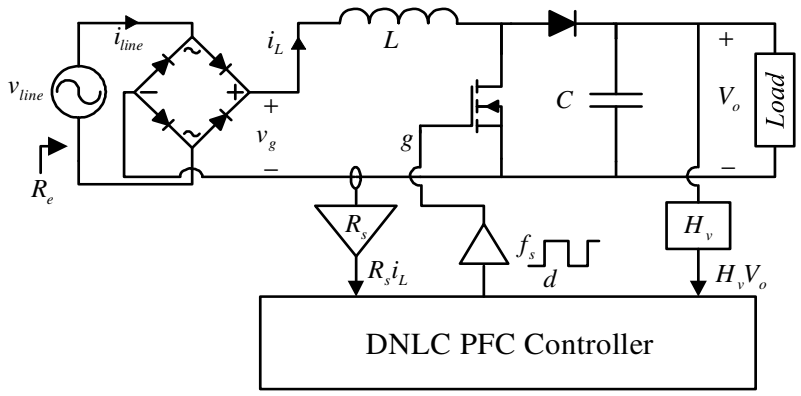


Figure 3.1: DNLC controlled PFC boost rectifier.

law. Section 3.2 describes the voltage regulation loop and addresses modeling of the outer voltage loop gain when a DNLC PFC controller is utilized. Section 3.3 discusses system implementation and quantization issues. Experimental results for a 300W boost DNLC PFC controlled rectifier are presented in Section 6.3.

3.1 Derivation of the Basic Digital Nonlinear Carrier PFC Control Law

With reference to Fig. 3.1, in a PFC rectifier the current control objective can be written as: $\langle i_L \rangle = v_g/R_e$, where v_g is the rectified line voltage, $\langle i_L \rangle$ is the low-frequency (average) component of the inductor current, and R_e is the emulated input resistance, $R_e = V_{g,rms}^2/P$, where P is the operating power of the PFC rectifier stage [7]. Using the quasi-static approximation, assuming v_g is changing slowly compared to the switching period T_s, for the CCM boost converter, $V_o(1-d) = v_g$, where d is the switch duty ratio, the current control objective can be expressed as

$$\langle i_L \rangle = \frac{V_o}{R_e}(1-d) = \frac{V_o P}{V_{g,rms}^2}(1-d) = \frac{1}{u}(1-d) \tag{3.1}$$

where

$$u = \frac{V_{g,rms}^2}{V_o P} = \frac{R_e}{V_o} \tag{3.2}$$

takes the role of a power control signal. In [14], the steps leading to (3.1) were followed by a discussion of analog modulator realizations aimed at implementing the PFC current control objectives

reformulated in terms of V_o and d. A different approach, better suited for digital implementation, follows by solving (3.1) for the duty cycle command $d[n]$ directly as a function of the current sample $i_L[n] = \langle i_L \rangle$, where $i_L[n]$ represents a sample of the inductor current ideally in the middle of the switch on-time, or in the middle of switch off-time, and u is the power control signal

$$d[n] = 1 - u i_L[n] \,. \tag{3.3}$$

Equation (3.3) is the basic version of the proposed DNLC current control law. Note that (3.3) requires no input voltage sensing or explicit compensation of the current control loop. As shown in Fig. 3.1, the DNLC controller presented in this chapter requires only current sensing and sensing of the output voltage. It is of interest to note that an alternative direction in pursuing simplified digital PFC control is taken in [42] where the input and the output voltage are measured using very simple A/D converters, while a current estimator removes the need for current A/D conversion. Fig. 3.2 shows experimental waveforms illustrating operation of a DNLC controller based on (3.3).

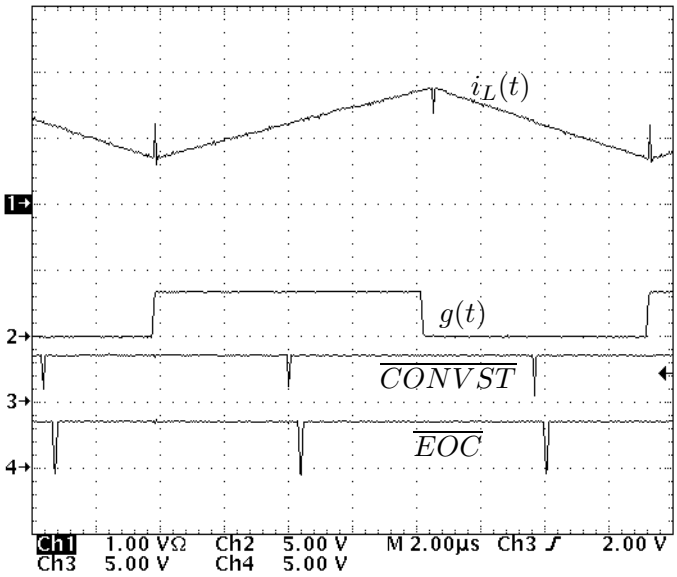
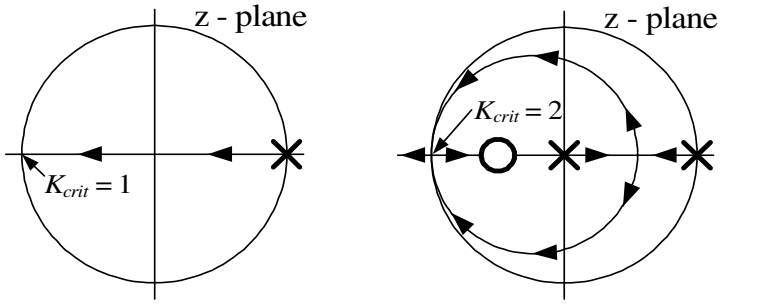


Figure 3.2: Experimental waveforms illustrating the operation of the boost PFC with DNLC PFC current control law (3.3).

The current A/D conversion start ($\overline{CONVST}$) and end of conversion ($\overline{EOC}$) signals show how the inductor current is sampled in the middle of the switch on-time or off-time (as in [16, 43]).

The timing of these signals is facilitated by the use of a triangle-wave DPWM. The current sample instance used to update the duty cycle command $d[n]$ by computing (3.3) is determined by the previous value of the duty cycle command, $d[n-1]$. If $d[n-1] > 0.5$ the on-time sample instance is used, otherwise the off-time sample instance is used. The implementation of this simple sample mode logic function effectively maximizes the allowable conversion time of the inductor current sensing A/D. The minimum required sampling rate of the inductor current sensing A/D is $\approx 4f_s$. During operation in either sample mode (on-time or off-time sampling), the duty cycle command $d[n]$ is updated immediately after either the respective on-time or off-time ($\overline{EOC}$) occurs.

3.1.1 Stability of the Current Control Loop



(a) Root-locus plot of $T_i(z)$ for the basic DNLC control law given in (3.3).

(b) Root-locus plot of $T_i(z)$ for the DNLC control law with a two sample current filter, $\alpha_1 = 0.75$ and $\alpha_2 = 0.25$.

Figure 3.3: Root-locus plots of closed loop system poles for two implementations of the DNLC PFC controller.

The small-signal stability of the current control law (3.3) is examined in this section starting from a discrete-time model based on both the quasi-static approximation, assuming that the input voltage, v_g, can be considered to be constant on the time scale of several switching periods, and the approximation that the output voltage, V_o, is constant and not time varying. From the large-signal relationship [43],

$$i_L[n+1] = i_L[n] + \frac{v_g}{L}T_s - \frac{V_o}{L}(1 - d[n])T_s\,, \tag{3.4}$$

a small-signal discrete-time relation yields the control-to-current transfer function

$$G_{id}(z) = \frac{\hat{i}_L(z)}{\hat{d}(z)} = \frac{V_o}{L}\frac{T_s}{z-1}\,. \tag{3.5}$$

Linearization of (3.3) gives the effective current-loop compensator transfer function

$$G_{ic}(z) = \frac{\hat{d}(z)}{\hat{i}_L(z)} = -u\,. \tag{3.6}$$

Combining (3.2), (3.5) and (3.6), the effective discrete-time current control loop gain is obtained

$$T_i(z) = -G_{id}(z)G_{ic}(z) = \frac{R_e T_s}{L}\frac{1}{z-1} = 2K_{crit}\frac{1}{z-1}\,, \tag{3.7}$$

where $K_{crit} = R_e T_s/2L$ is a parameter that determines the operating mode (CCM or DCM) of the boost converter in the PFC rectifier [7]. Based on (3.7), stability of the current control loop can be examined using root-locus techniques with K_{crit} as a gain parameter, as shown in Fig. 3.3(a). The root-locus given shows that the current loop is stable (i.e. has a pole inside the unit circle) as long as $K_{crit} < 1$, which is the same condition that characterizes the boost PFC rectifier operating in CCM over the entire line cycle [7]. In conclusion, the current loop based on (3.3) is small-signal stable at high power levels when the converter always operates in CCM during the entire line cycle. At reduced power levels, the boost converter operates in DCM around the zero crossings of the ac line, and in CCM around the peak of the ac line. Instability of the current loop during a CCM operation section of a mixed-mode (DCM and CCM) line period typically manifests itself as current period-doubling. This type of bounded oscillatory behavior results in increased line current total harmonic distortion (THD), which may be tolerated. It is nevertheless of interest to investigate modifications of the current control law to achieve stable operation in CCM at lighter loads, i.e. for larger values of K_{crit}. In particular, the addition of control law dynamics through the inclusion of a current filter prior to the calculation of the duty cycle via (3.3) is considered. In these cases $i_L[n]$ in (3.3) is replaced by a filtered current, $i_{L,filtered}[n]$ that is calculated by

$$i_{L,filtered}[n] = \alpha_1 i_L[n] + \alpha_2 i_L[n-1] + \cdots + \alpha_k i_L[n-(k-1)]\,, \tag{3.8}$$

where $\alpha_1, \alpha_2, \ldots, \alpha_k$ are the implemented filter coefficients. The filter coefficients (α's) that provide the highest CCM stable K_{crit} in closed loop for a given filter order are given in Table 3.1. The

coefficients for the current filters comprised of only two or three current samples were found by visual inspection of the closed loop root-locus plots, generated numerically, followed by small adjustments to filter coefficients. For higher order filters an evolutionary algorithm [44] was employed to determine the optimal filter coefficients. A detailed description of the evolutionary algorithm used to determine optimal higher order filter coefficients is provided in Appendix A. Additionally, Table A.1 shows the solved filter coefficients for current filters having up to eight coefficients.

Table 3.1: Current filter coefficients for extending the K_{crit} stability range of the DNLC PFC controller.

K_{crit}	Current Filter Coefficients				
Realized	α_1	α_2	α_3	α_4	α_5
1.000	1.000	-	-	-	-
2.000	0.750	0.250	-	-	-
3.000	0.554	0.333	0.113	-	-
4.000	0.439	0.314	0.186	0.061	-
5.000	0.364	0.285	0.200	0.114	0.037

As Table 3.1 shows, all filter coefficients sum to one as to not change the current sensing dc gain. Also, all coefficients are monotonically decreasing with higher order. The maximum stable K_{crit} is increased by 1 for every added order of the current filter. The root-locus plot for the current filter with two current samples is shown in Fig. 3.3(b). The plot indicates that the current loop is stable for $K_{crit} < 2$. This effectively extends the range of stable CCM operation from $K_{crit} < 1$ to $K_{crit} < 2$ compared to the basic DNLC PFC control law given in (3.3). The filter coefficients for the two sample current filter are also easily implemented in a digital system without the need for additional hardware multipliers as the filter coefficients can be implemented by simple bit shifts and additions. Due to the ease of implementation and increased CCM stability range, the DNLC PFC control law with an implemented two sample current filter was selected for implementation in the experimental prototype.

3.1.2 Operation and Stability at Light Loads

During light load operation the converter will operate in DCM during some portion or all of the input voltage line cycle and the power command signal u will be limited to its maximum stability limit u_{max}, found as

$$u_{max} = \frac{2K_{crit}L}{V_o T_s}\,, \tag{3.9}$$

where K_{crit} is determined based on the stability criterion discussed in Section 3.1.1. To maintain voltage regulation in light load conditions when the traditional power command signal has reached the stability boundary, $u = u_{max}$, a further modification is made to the basic DNLC current control law (3.3),

$$d[n] = d_{max} - u i_L[n]\,, \tag{3.10}$$

where d_{max} is a secondary power command signal that represents the maximum allowable duty cycle during any given half line period. This modification effectively implements the basic DNLC current control law given in (3.3) with a duty cycle command offset equal to $(1 - d_{max})$ that is adjusted to maintain output voltage regulation. During higher power operation, when $u < u_{max}$, d_{max} is equal to 1, thus reducing the control law given in (3.10) back to (3.3). This modification makes voltage regulation possible down to essentially zero load even for high input voltage levels, at the expense of somewhat increased input current distortion at light loads.

3.2 Voltage Regulation and Power Control

A block diagram of a boost rectifier with the complete DNLC PFC controller is shown in Fig. 3.4. Based on the sampled output voltage error, the voltage loop compensator, $G_{cv}(z)$, computes the power control signal $y[k]$. During operation at high power levels and lower line voltages $u[n] = y[k]$. However, as the operating power level is reduced, $u[n]$ is limited to a value of u_{max} as described in the previous section. The power command signal, $y[k]$, then continues to increase initiating a reduction of $d_{max}[k]$ via the d_{max} control loop. The discrete time sample instances in the voltage loop are denoted using the letter k as opposed to the letter n to denote a

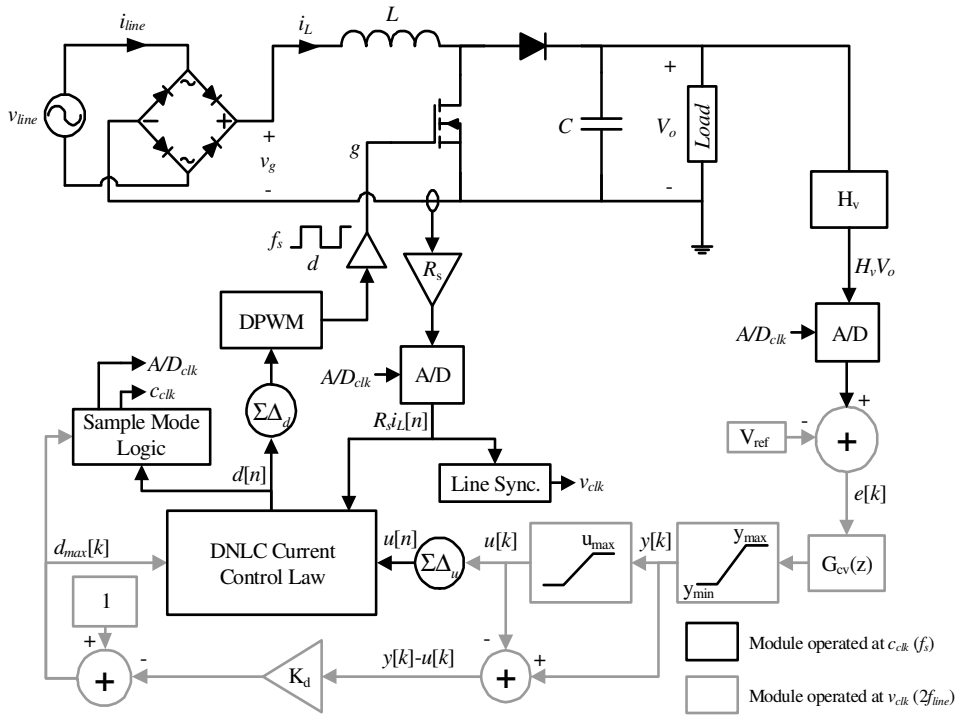


Figure 3.4: Complete DNLC PFC controller.

difference in sample frequency. As the bandwidth of the outer voltage loop must be low, at least during steady-state operation, it is advantageous to sample the output voltage at a rate synchronous to $2f_{line}$. Benefits of sampling at this rate include the fact that input current harmonic distortion is unaffected by the output voltage ripple and that voltage loop limit cycling can be avoided as described in [45]. Furthermore, a satisfactory outer voltage loop PI compensator can be realized using less hardware compared to a similar performance PI compensator designed with a sample rate of f_s due to shortened register lengths required to implement the compensator. The requirement for synchronization to the ac line is provided by generating a clock derived from a digital comparison of either the sensed inductor current or duty cycle command with a constant. The generation of the voltage loop clock, v_{clk}, is shown in Fig. 3.4 as the Line Sync. block. Line synchronization could also be provided by the output voltage loop itself through the use of the single comparator A/D approach [46].

3.2.1 Power Control via $u[n]$

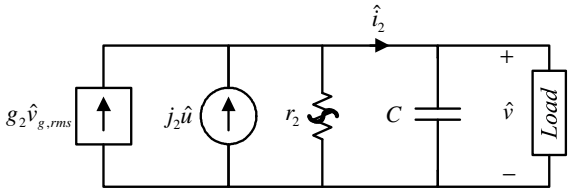


Figure 3.5: Averaged small signal model of the DNLC controlled boost PFC output port.

Fig. 3.5 shows a continuous time low-frequency small-signal model of the PFC output stage obtained by averaging over a half line cycle [7] for the DNLC PFC current control law described in Section II when the boost PFC stage operates in CCM during the entire line period. Small-signal perturbations of the power command signal, PFC output port current, and rectifier output voltage are denoted by $\hat{u}$, $\hat{i_2}$ and $\hat{v}$ respectively. This model is valid for frequencies below $2f_{line}$ and assumes a constant operating point. During CCM always operation $u[n] = y[k]$ (as $u[n] < u_{max}$) and $u[n]$ and the emulated input resistance (R_e) are related by (3.2). Under these operating conditions the small-signal model parameters are

$$j_2 = -\frac{P^2}{V_{g,rms}^2} \tag{3.11}$$

and

$$r_2 = \frac{V_o^2}{2P}\,, \tag{3.12}$$

where P is the average operating power of the PFC rectifier stage. The input voltage gain, g_2, is omitted from calculation because $\hat{v}_{g,rms} = 0$ when computing the small-signal control-to-output gain, $\hat{u}$ to $\hat{v}$. Assuming a resistive load of value $R = V_o^2/P$, solving the model results in the control-to-output transfer function for the DNLC PFC controlled boost rectifier

$$G_{vu}(s) = \frac{\hat{v}(s)}{\hat{u}(s)} = \frac{-PV_o^2R_s}{3V_{g,rms}^2}\left(\frac{1}{1+sCR/3}\right) = G_{vy0}\left(\frac{1}{1+s/\omega_p}\right)\,. \tag{3.13}$$

This single pole plant transfer function is easily compensated with a linear PI compensator, $G_{cv}(z)$ in Fig. 3.4, in order to achieve a standard slow voltage loop control bandwidth of $\approx$ 10Hz and

a phase margin of $\approx 70^\circ$ under the highest expected dc loop gain conditions. Load transient responses for a DNLC controlled PFC rectifier with similar power stage parameters to those given in Table 3.2 and a nearly identical digital voltage loop implementation to the one described here are shown in [46].

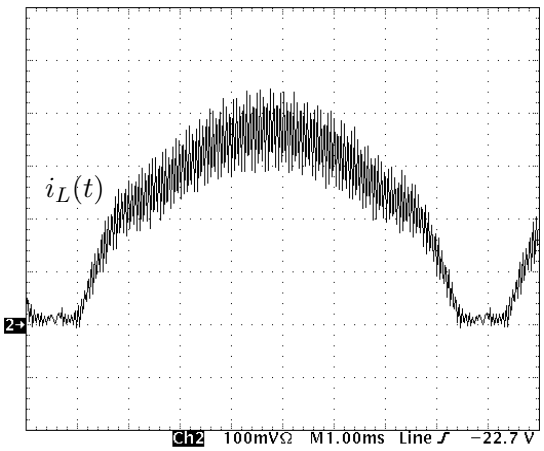
3.2.2 Power Control via $d_{max}[k]$

During rectifier operation at lower power levels and/or higher input voltages the stage operates in DCM during some or all of the input voltage line cycle. During this type of operation $u[n]$ is saturated at u_{max} and the power is controlled via the d_{max} control loop defined by

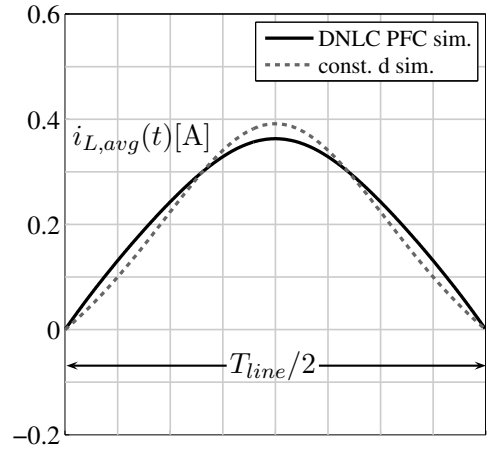
$$d_{max}[k] = 1 - K_d(y[k] - u_{max})\,, \tag{3.14}$$

where K_d is a linear gain term that relates the unsaturated power command signal, $y[k]$, and the secondary power command signal, $d_{max}[k]$. In order to fully design the outer voltage loop by specifying K_d, it was of interest to investigate the expected dc gain of the implemented DNLC PFC controller during CCM/DCM mixed mode and DCM always operation. Under these operating conditions the PFC rectifier inductor current is distorted from the ideal rectified sine waveform due to several factors: implementation of a CCM derived control law as shown in (3.3), a duty cycle command offset applied to this law in order to maintain output voltage regulation as shown in (3.10), and inaccurate sensing of the average inductor current during DCM operation. In DCM the average inductor current is either over-estimated during on-time sampling or under-estimated during off-time sampling. The expected input current distortion due to these many factors indicates that the emulated input resistance, R_e, of the PFC rectifier is not constant over a half line cycle period which precludes the use of the averaged small-signal model output port model shown in Fig. 3.5 which assumes a constant R_e over a half line cycle period. As there is no closed-form analytical link between $y[k]$ and R_e for the implemented controller, a numerical simulator was used to calculate the expected average power processed during each half line cycle period given the implemented control law (3.10) and the outer voltage loop control topology shown in Fig. 3.4.

Additionally, inspection of (3.10) shows that the implemented controller law becomes equivalent to a constant duty cycle controller as the sensed inductor current decreases ($i_L[n] \to 0$). In this case, the analytical model developed in [47] applies, and provides a guide for an initial selection of the gain parameter K_d. However, in the absence of a comprehensive analytical model, numerical simulations were necessary to evaluate operation in mixed CCM/DCM and DCM only modes.



(a) Inductor current waveform collected using the DNLC PFC controller.

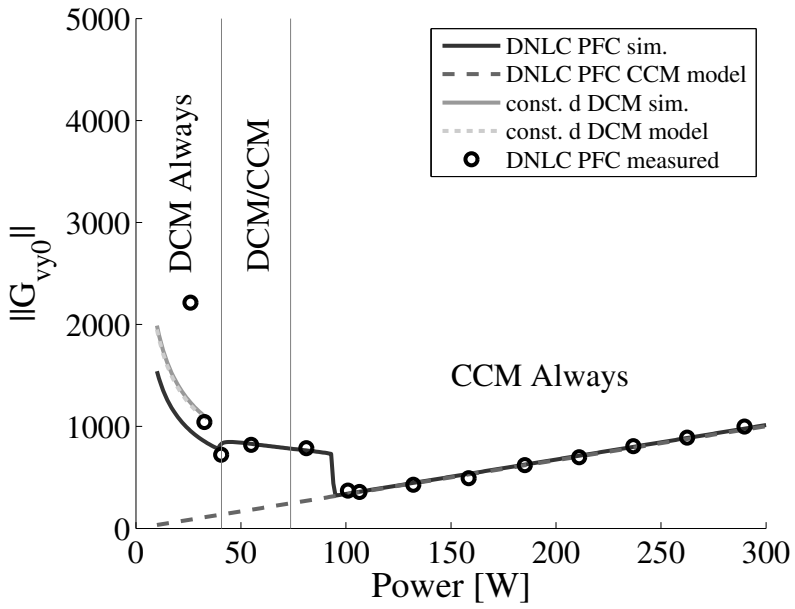


(b) Inductor current waveforms computed using the DNLC PFC simulator and the constant duty cycle controller simulator.

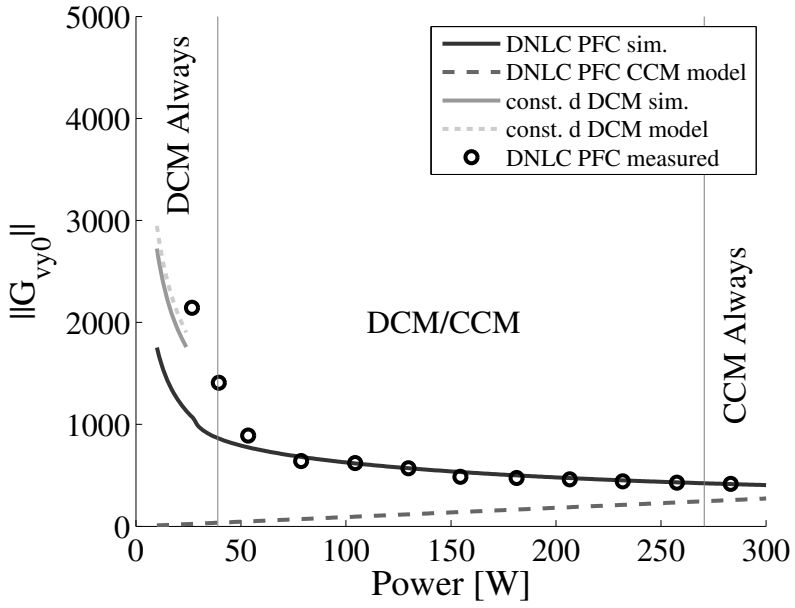
Figure 3.6: Comparison of experimental and simulated inductor current waveforms in DCM always operation, $P = 30$W, $V_{g,rms} = 120$V, 60Hz.

Figs. 3.6(a) and 3.6(b) respectively show an experimental inductor current waveform collected at an operating power of 30W and a rms input voltage of 120V, 60Hz, and the corresponding simulated average current waveforms produced by both the DNLC PFC simulator and the constant duty cycle control simulator. Disregarding the experimental inductor currents zero-crossing distortion, the experimental waveform shows characteristics of both simulated controller techniques. At low current levels the inductor current rises sharply as the duty cycle command is fixed at $d_{max}[k]$. At higher current levels the sensed inductor current reduces the duty cycle command via (3.10) and results in a higher quality current waveshape than attainable with a constant duty cycle controller alone.

The simulators were further employed to determine the dc control-to-output transfer func-



(a) $V_{g,rms} = 120$V, 60Hz, $K_d = 2.0$.



(b) $V_{g,rms} = 230$V, 50Hz, $K_d = 2.0$.

Figure 3.7: Control-to-output transfer function dc gains of the outer voltage loop for $V_{g,rms} = 120$V, 60Hz, and 230V, 50Hz, and d_{max} control gain $K_d = 2.0$, basic DNLC PFC control law given by (3.3), $u_{max} = 0.4$.

tion gain as a function of operating power level, rms input voltage and d_{max} control gain K_d. Figs. 3.7(a) and 3.7(b) show the resulting dc transfer function gains for $V_{g,rms}$ = 120V, 60Hz and 230V, 50Hz, respectively and a K_d = 2.0. The figures also show experimentally measured dc control-to-output gains and two computed control-to-output dc gains from analytical models. The first is the dc gain (G_{vy0}) from (3.13). The second (labeled as "const. d DCM model" in Figs. 3.7(a) and 3.7(b)) is from the analytical constant duty cycle control model [47] that is valid during DCM always operation.

In Fig. 3.7(a) the point at which $u[n]$ saturates at u_{max} is clearly visible at approximately 95W. This transition from $u[n]$ control to $d_{max}[k]$ control does not occur exactly at the mixed mode CCM/DCM and CCM always boundary because of an implemented stability safety margin on u_{max} (see Section 3.3.1). Prior to this transition the simulated, modeled and measured control-to-output dc gains are all in close agreement. In the DCM always region the simulated, modeled and measured gain are also closely matched verifying that the DNLC PFC controller is approximately a constant duty cycle controller at very low powers. At a higher line voltage, as in Fig. 3.7(b), the DNLC PFC controller operates under $d_{max}[k]$ control over the entire power range. Again at low powers the measured dc gain closely matches the gain expected from a constant duty cycle controller [47]. These control-to-output dc gains are specific to the prototype described. Different boost inductances and/or converter operating frequencies will result in different control-to-output transfer function dc gain characteristics by shifting the mode transition boundaries (CCM→DCM/CCM and DCM/CCM→DCM) to higher or lower operating power levels.

The effect of changing the d_{max} loop design parameter, K_d, is shown in Fig. 3.8. The DNLC PFC simulator, measured, and DCM constant duty cycle controller gains are shown for K_d = 2.0 and 0.5. It is clearly shown that K_d linearly scales the dc gain curves when the d_{max} loop is active. Furthermore, Fig. 3.8 shows that the choice of K_d determines the low power gain characteristics of the DNLC PFC controller. For the prototype stage tested a K_d of 2.0 gives an increasing control-to-output dc gain as the operating power level decreases below about 95W. However the dc gain at 10W (P_{min}) is approximately equal to the gain expected in CCM always operation at a maximum

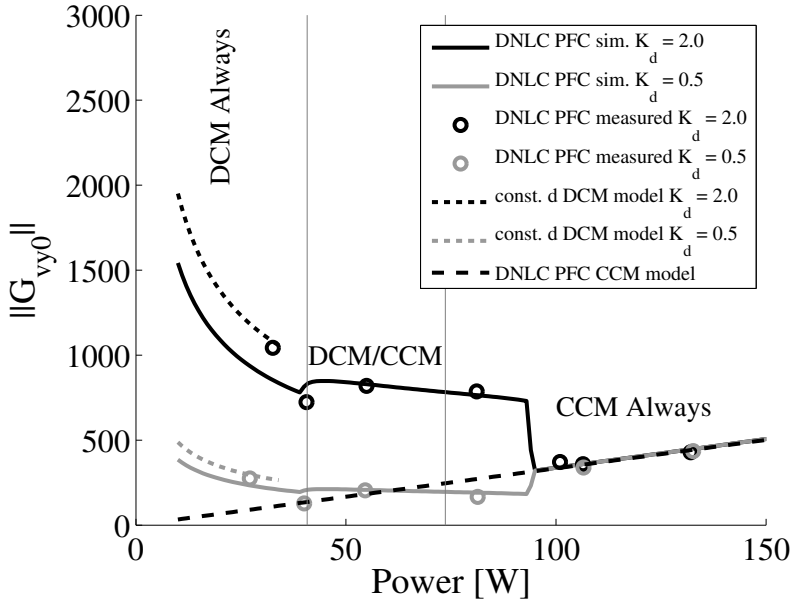


Figure 3.8: Outer voltage loop control-to-output dc transfer function gain for $V_{g,rms} = 120$V, 60Hz, and d_{max} control loop gains of $K_d = 2.0$ and 0.5.

output power of 300W. If the 300W DNLC PFC prototype were required to meet the PFC no limit cycling criteria given in [45], a K_d of 2.0 would generally provide a faster transient response when operating under d_{max} control compared to a K_d of 0.5 because the gain profile when $K_d = 2.0$ has less gain variation across the operating power spectrum and has nearly the same maximum gain at upper and lower power limits.

3.2.3 ΣΔ Modulation of $u[n]$

In the interest of minimizing the amount of hardware required to implement the DNLC PFC controller, it is beneficial to reduce the word size for the power command, $u[n]$, as it is directly multiplied with $i_L[n]$ or $i_{L,filtered}[n]$ in the DNLC PFC controller block. Reducing the word size of $u[n]$ allows for the use of a smaller digital multiplier and reduces the number of gates required to implement the DNLC PFC control law. However, at certain power levels the power differential between a 1 LSB step in $u[n]$ may become considerably large as shown in Figs. 3.7(a) and 3.7(b). Given the large oversampling ratio of $u[n]$ to $y[k]$ ($f_s/2f_{line}$), ΣΔ modulation can be very effective

in improving the effective resolution of the power command $u[n]$, with minimal hardware overhead. In the implemented DNLC PFC controller, a simple, first-order $\Sigma\Delta$ modulator ($\Sigma\Delta_u$ in Fig. 3.4) in the "error-feedback" configuration [48] shown in Fig. 3.9 is used to effectively represent a 10-bit (n_{in}) $u[n]$ using only an 8-bit (n_{out}) word size.

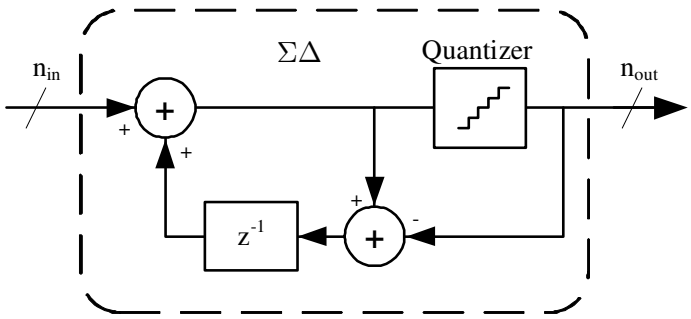


Figure 3.9: Error-feedback configuration of a first-order $\Sigma\Delta$ modulator.

3.3 System Implementation

The experimental prototype consists of a boost rectifier power stage and a digital controller implemented using a Xilinx FPGA development platform with a clock rate of 66.66MHz. The digital controller allows experimentation with the bit resolutions of the current sensing A/D (maximum inductor current resolution: $\approx$ 30mA) and voltage sensing A/D (maximum output voltage resolution: $\approx$ 2V) through the adjustment of the number of bits truncated from the native A/D bit resolution. Both A/Ds are implemented using commercially available, relatively low-cost 8-bit devices (Analog Devices AD7288) allowing a maximum sample rate of 2MHz. In a custom-IC implementation of the DNLC PFC controller a single multiplexed A/D could be utilized. The digital pulse-width modulator resolution (maximum resolution: 9-bits) was also adjustable via a communications port interfaced with the FPGA. Table 3.2 lists the power stage parameters for the DNLC controlled PFC prototype constructed.

Table 3.2: Prototype DNLC PFC parameters.

$V_{g,rms}$ range	85-265V
$V_{o,nominal}$	380V
L	1.5mH
C	220μF
f_s	65kHz
$P_{load,max}$	300W
Transistor	STP25NM60N
Diode	CSD04060

3.3.1 DNLC PFC Current Controller Bandwidth

The effective closed-loop bandwidth of the DNLC PFC control law is examined by constructing the Bode plot of the DNLC PFC loop gain given in (3.7) for two values of the steady state power command signal, $u = 0.8u_{max}$ and $u = u_{min}$ and for two controller cases from Section 3.1.1: the basic controller using a single current sample, and the controller with filtered current using two samples with coefficients shown in Table 3.1. Fig. 3.10 shows the loop gain magnitude and phase responses over a frequency range from 400Hz to $f_s/2$. Here, u_{min} is the power command signal value when operating at full power with an rms input voltage of 85 V. The worst-case (minimum) cross-over frequency, which is approximately equal to the closed loop bandwidth of the current control loop, occurs at u_{min}, and is approximately 2.5kHz (or approximately $f_s/25$). Operation with a power command of $0.8u_{max}$ gives cross-over frequencies of approximately 19kHz and 25kHz (or approximately $2f_s/5$), for the basic and the two sample current filter versions of the DNLC PFC control law, respectively. Quality of the resulting current waveshapes, presented in Sections 3.3.2 and 6.3 provide further evidence that the bandwidth of the current control loop can be considered adequate for the PFC application.

It should be noted that the discussion here is based on the simple discrete-time model of Section 3.1.1, which assumes constant output voltage. For analog PFC controllers based on (3.1), a more comprehensive study of the current loop bandwidth and interactions with the output filter capacitor dynamics and ripple has been presented in [49], where it was concluded that effects of the

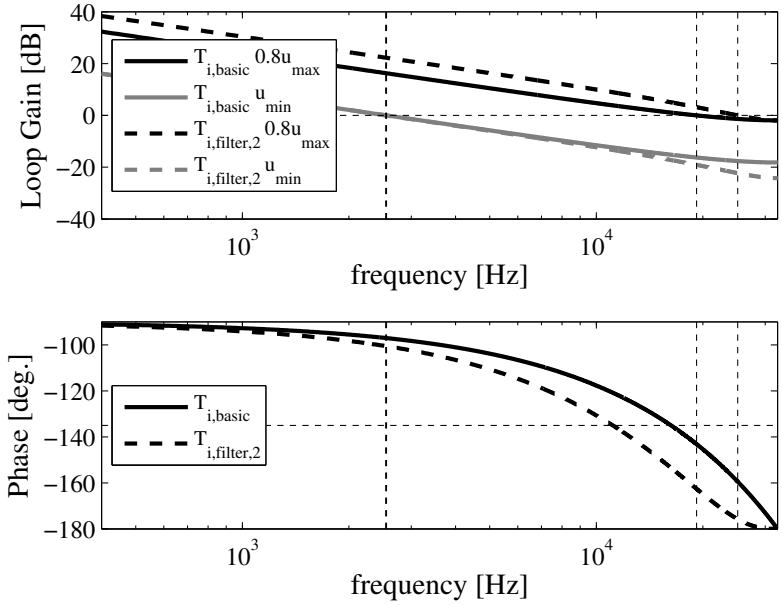


Figure 3.10: Current loop gain magnitude and phase of the basic DNLC control law given in (3.3) and the two sample current filter DNLC control law at steady state operating power levels corresponding to u_{min} and $0.8u_{max}$ for a PFC rectifier with power stage parameters given in Table 3.2.

output voltage ripple are relatively minor from the practical point of view, and that the bandwidth of the considered analog current control loop should suffice in practical PFC applications.

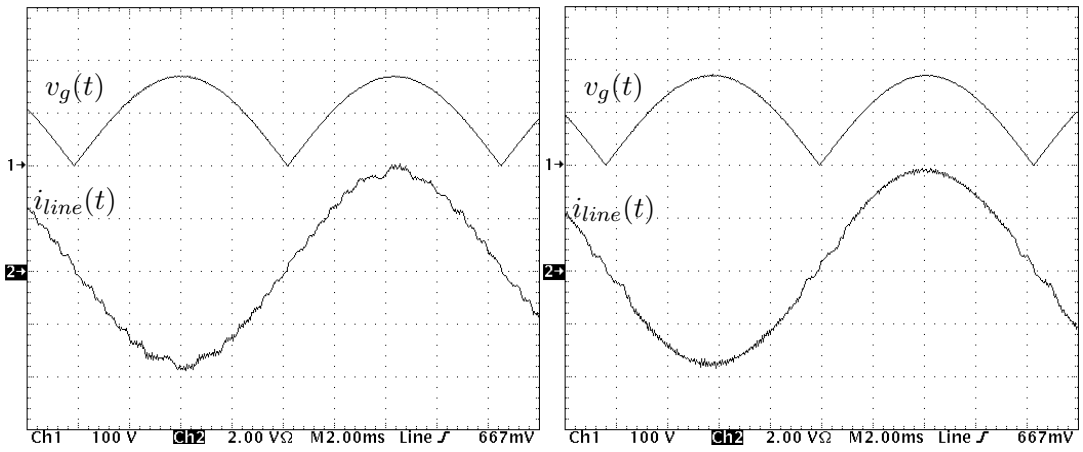
3.3.2 Quantization issues

An objective was to meet EN 61000-3-2 Class D standards [1] with the simplest digital implementation possible to yield a cost effective digital PFC controller and reduce the number of connections needed to interface the controller. The effects of various resolutions of the DPWM and the current sensing A/D were investigated to this aim.

3.3.2.1 DPWM Resolution

The resolution of the DPWM was variable from 1-bit to 9-bits. During experimentation it was determined that the 1-bit and 2-bit settings were simply not feasible and produced extreme quantization effects. Implementing a first-order $\Sigma\Delta$ modulator ($\Sigma\Delta_d$ in Fig. 4) to modulate the

duty-cycle command $d[n]$ allows the DPWM resolution to be lowered to as low as 3-bits while maintaining EN 61000-3-2 Class D current harmonic limit standards at a 300W power level. A DPWM setting of 4-bits, with $\Sigma\Delta$ modulation of an additional 5 LSBs is a suitable setting for the operation of the boost PFC over the entire range of input voltages and output power levels. Reducing the DPWM resolution from 9-bits to 4-bit allows the digital logic clock rate of the DPWM module to be reduced from 66.66MHz to 2.08MHz. With this DPWM clock rate reduction, the clock rate for the overall controller can also be significantly reduced depending on the digital clock rate required by the implemented A/Ds.



(a) $\Sigma\Delta_d$ modulation disabled.

(b) $\Sigma\Delta_d$ modulation enabled, 5 LSBs in error feedback.

Figure 3.11: Converter waveforms with and without $\Sigma\Delta$ modulation of the duty cycle command enabled, $P = 300$W, $V_{g,rms} = 120$V, 60Hz, 4-bit DPWM, 8-bit current sensing A/D.

Fig. 3.11 shows line current waveforms with and without $\Sigma\Delta$ modulation of the 4-bit duty cycle command signal with a full current sensing A/D resolution of 8-bits at $P = 300$W and $V_{g,rms} = 120$V, 60Hz. Fig. 3.11(a) shows the line current waveform when $\Sigma\Delta_d$ is disabled. No low frequency limit-cycling is present, due to a high effective resolution of $u[n]$ but the line current clearly shows a stair-step like appearance due to the quantization of $d[n]$. With $\Sigma\Delta_d$ enabled, Fig. 3.11(b) shows a smooth $i_{line}(t)$ waveform that easily meets harmonic current specifications.

3.3.2.2 Current Sensing A/D Resolution

Table 3.3: THD measurements for various current A/D resolutions, 9-bit DPWM, $P = 300$W.

Current A/D Resolution		$V_g = 120$V, 60Hz	$V_g = 230$V, 50Hz
(bits)	mA/bit	THD(%)	THD(%)
8	30	3.9	4.8
7	61	4.0	5.3
6	122	4.3	5.8
5	244	4.7	5.7
4	488	6.8	9.4
3	975	7.5	14.2

The current sensing A/D had a variable resolution of 3-bits to 8-bits. Table 3.3 shows how the current sense resolution affects the THD of the line current. The increase in the THD at low current A/D resolutions is due to increased zero-crossing distortion due to a larger zero current bin and a stair-step like current wave-shape producing harmonics at many multiples of the fundamental. The DPWM resolution was set to a full 9-bits of resolution in order to demonstrate the effects of the current sensing A/D resolution apart from other DPWM resolution effects. The current sensing resolution in mA/bit is also presented in Table 3.3. For the 3-bit current sensing A/D the current LSB quantization step is nearly 1A. Nevertheless, at 300W the EN 61000-3-2 Class D harmonic current limits are not exceeded.

3.3.2.3 Combined Quantization Effects

The combined effects of current sensing A/D resolution and DPWM resolution with and without $\Sigma\Delta$ modulation were investigated for a near minimal hardware configuration. Fig. 3.12 is a plot of the power normalized harmonic current magnitudes for the same conditions as shown in Fig. 3.11. Normalized harmonic current magnitudes are shown for converter operation with and without $\Sigma\Delta$ modulation of the duty cycle command enabled. The EN 61000-3-2 Class D odd harmonic current limits, scaled for low line voltage operation, are also shown. Without the $\Sigma\Delta_d$ block active the controller operating with a 3-bit DPWM is still capable of passing the harmonic

current limits although the amplitude of the 15$^{\text{th}}$ harmonic is quite close to surpassing the harmonic current limit standard. With the duty cycle command $\Sigma\Delta$ modulator enabled, with 6 LSBs of error feedback, the 3-bit DPWM easily passes the harmonic current limits. Furthermore, Fig. 3.12 shows that the $\Sigma\Delta_d$ block is capable of distributing low frequency current harmonics to higher frequencies. For instance, the 3$^{\text{rd}}$ harmonic is reduced using the $\Sigma\Delta$ modulator; however, more harmonic current is seen in the 5$^{\text{th}}$ harmonic current than without $\Sigma\Delta$ modulation. The overall effect is a redistribution of harmonic currents to higher harmonic orders.

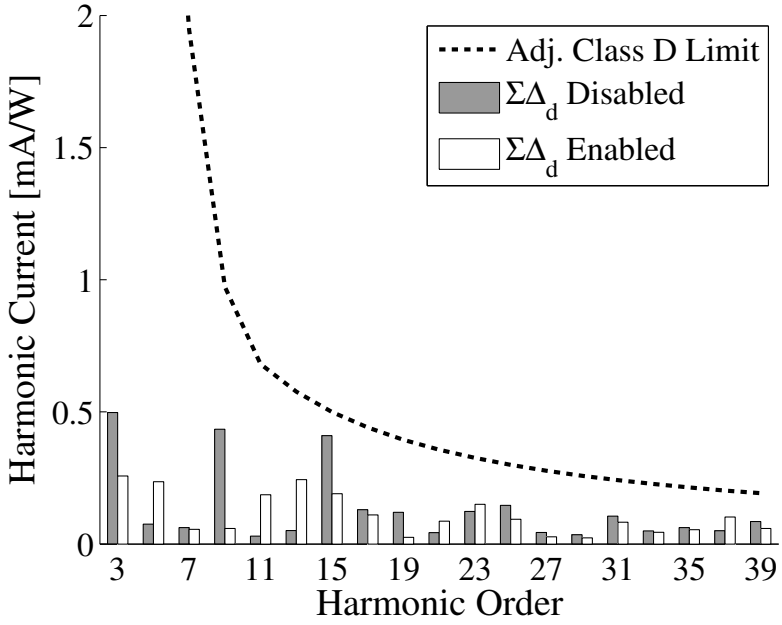
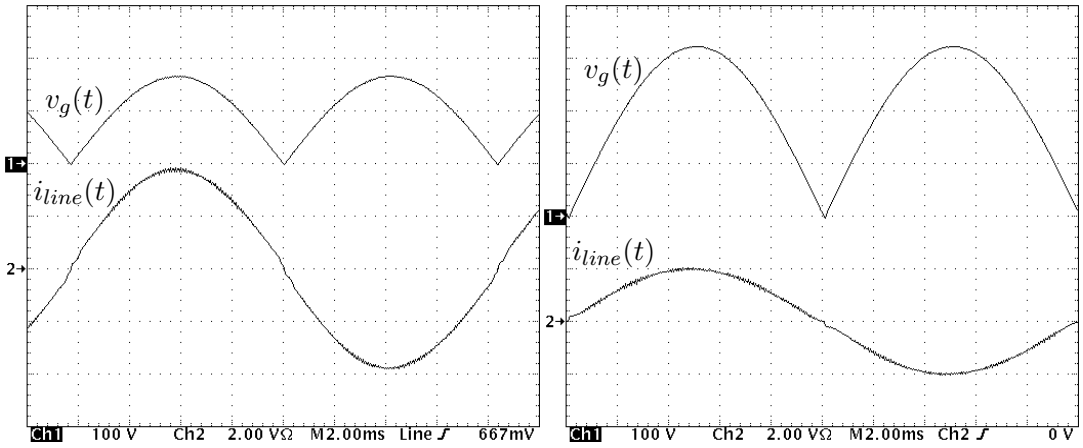


Figure 3.12: Harmonic current levels with and without $\Sigma\Delta_d$ dithering implemented, $P = 300$W, $V_{g,rms} = 120$V, 60Hz, 3-bit DPWM, 4-bit current sensing A/D.

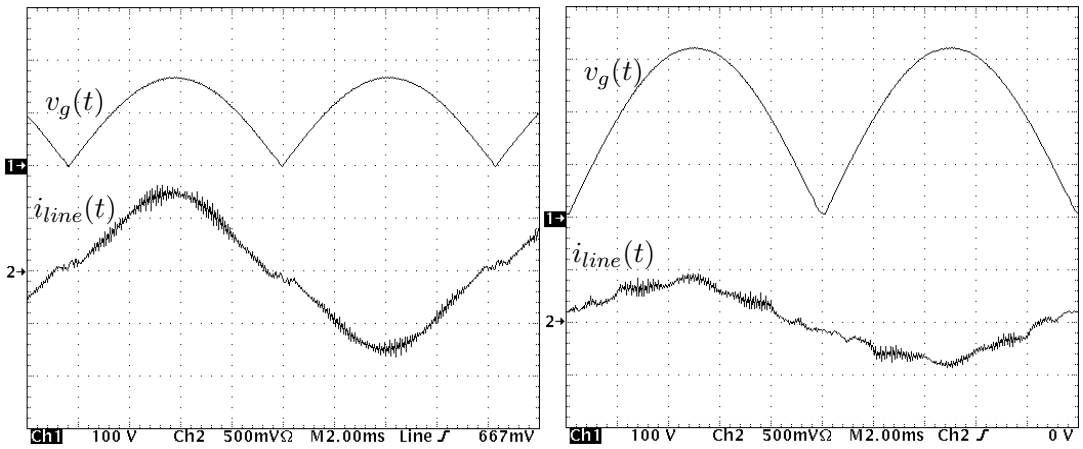
3.4 Experimental Waveforms

3.4.1 Operation at High and Moderate Power

Fig. 3.13 shows the experimental rectified line voltage, $v_g(t)$, and line current, $i_{line}(t)$, waveforms for nominal line voltages of 120V, 60Hz, and 230V, 50Hz, and operating power levels of 300W and 50W. The implemented DPWM has a 4-bit resolution and the current sensing A/D has



(a) $V_{g,rms} = 120$V, 60Hz, $P = 300$W (b) $V_{g,rms} = 230$V, 50Hz, $P = 300$W



(c) $V_{g,rms} = 120$V, 60Hz, $P = 50$W (d) $V_{g,rms} = 230$V, 50Hz, $P = 50$W

Figure 3.13: Experimental DNLC PFC waveforms, $i_{line}(t)$ and $v_g(t)$, for $P = 300$W and 50W, $V_{g,rms} = 120$V, 60Hz and 230V, 50Hz, 4-bit DPWM, 8-bit current A/D.

a resolution of 8-bits. The duty cycle command is $\Sigma\Delta$ modulated with 5 LSBs in error feedback. The implemented complete DNLC PFC controller requires roughly 3,000 equivalent logic gates. At all operating points the line current shaping has the characteristics of high power factor and low THD particularly at full operating power, $P = 300$W, when the converter is in CCM operation for the entire line cycle. The EN 61000-3-2 Class D harmonic current limits are met for all specified operating conditions.

Table 3.4 shows the measured power factor (PF) of the DNLC controlled PFC at 100%, 50%

Table 3.4: Power factor measurements for the DNLC PFC with a 4-bit DPWM with a 5-bit $\Sigma\Delta_d$ and an 8-bit current A/D.

P_{load}	Measured PF		Minimum PF Specification	
[%]	(120V)	(230V)	80 Plus (120V)†	80 Plus (230V)†
100%	0.999	0.996	-	-
50%	0.998	0.980	0.9	0.95
20%	0.987	0.934	-	-

† Specifications are for the highest certification category available.

and 20% load for line voltages of 120V, 60Hz, and 230V, 50Hz. The specified power factor minimums for the 80 Plus certification program is also listed. For both input voltage cases, the DNLC PFC exceeds the minimum power factors required for certification with a considerable margin.

3.4.1.1 Operation at Very Low Power

Fig. 3.14 shows the converter waveforms at a line voltage of 230V, 50Hz, and an operating power of 20W. The converter output is still regulated and the line current is reasonably shaped although current THD is increased to 28.6%.

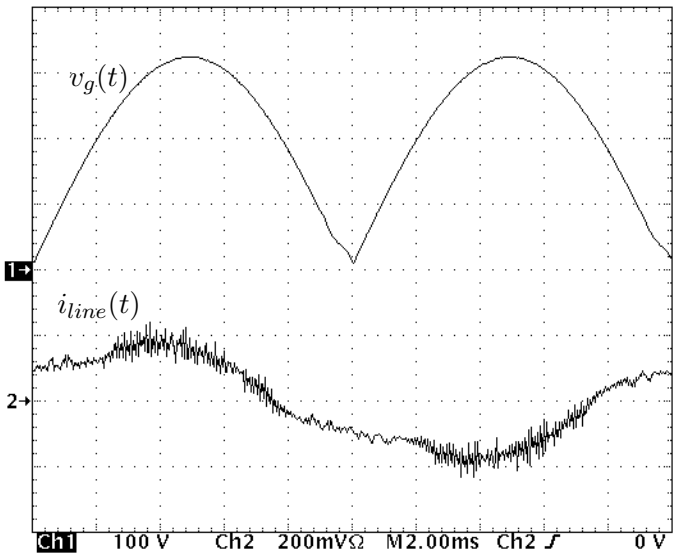


Figure 3.14: Converter waveforms for very light load operation, $P = 20$W, $V_{g,rms} = 230$V, 50Hz, 4-bit DPWM and current sensing A/D.

3.5 Chapter Summary

This chapter introduces a digital non-linear carrier (DNLC) PFC control approach that requires no input voltage sensing or explicit current loop compensation, yet results in low-harmonic operation over a universal input voltage range and operating power levels from high-load operation in continuous conduction mode down to near-zero load in discontinuous conduction mode. The controller architecture, together with simple first-order $\Sigma\Delta$ modulation blocks for control signals, enable the DNLC PFC controller to be realized with a low-resolution DPWM, low resolution A/D converters and a low clock rate. The DNLC controller is suitable for stand-alone low-cost custom-IC implementation, or as a hardware description language (HDL) module well suited for integration with other power control and power management functions. Experimental verification results are shown for a 300W boost DNLC PFC rectifier.

Chapter 4

Quantization Effects and Limit Cycling in Digitally Controlled Single-Phase PFC Rectifiers

This chapter examines quantization effects and limit cycling in the voltage control loop of digitally controlled single-phase power factor correction (PFC) rectifiers. Low-frequency limit cycling in the voltage loop can result in undesirable dc components, even harmonics in the ac line current and flicker. It is shown that two mechanisms can result in low-frequency limit-cycling: nonsynchronous sampling of the output voltage and quantization of the power command signal. Conditions for avoiding limit cycling are presented and verified in simulations and experiments on digital average current mode (DACM) and digital non-linear carrier (DNLC) controlled PFCs.

In the area of digitally controlled single-phase power factor correction (PFC) rectifiers, such as the boost PFCs in Figs. 4.1 and 4.2, much attention has been given to the design and implementation of the current shaping loop, improvement of the dynamic response of the voltage control loop, and minimization of hardware requirements [15–17, 20, 21, 37, 39, 40, 50–52]. However, with the exception of a brief discussion in [17], quantization effects and potentials for low-frequency limit cycling oscillations in the voltage control loop have not been addressed.

In digitally controlled boost PFCs, quantization of the output voltage error leads to quantization of the power command signal. As a result, the output power of a digitally controlled rectifier can only be adjusted in discrete power increments. A mismatch between the PFC output power and the load power can result in low-frequency variations (limit cycling) of the output voltage and the input current amplitude. As PFC's have a considerable amount of output voltage ripple

at twice the line frequency ($2f_{line}$), due to the inherent instantaneous power imbalance between the converter input and output, any additional subharmonic ripple due to limit cycling can be considered negligible. However, when the boost PFC input current with low-frequency variations in amplitude is unfolded by the input diode bridge, such low-frequency limit cycling can result in highly undesirable dc current, even harmonics in the ac line current (i_{line}) and flicker.

Quantization effects have been studied in the area of digitally controlled DC-DC converters [53,54], where the origins of limit cycling oscillations and design criteria to avoid such disturbances have been formulated in terms of resolutions of the voltage-sensing A/D converter and the digital pulse-width modulator (DPWM), and control loop parameters. The objectives of this chapter are to examine the quantization effects and discuss no limit-cycling conditions for the voltage control loop in digitally controlled PFC rectifiers.

Section 4.1 briefly reviews control architectures and operation of the digitally controlled boost PFC rectifiers using either a digital average current mode (DACM) (Fig. 4.1) or digital non-linear carrier (DNLC) PFC controller (Fig. 4.2), and the corresponding large-signal model in Fig. 4.3. Two main mechanisms through which limit cycling can occur in the PFC voltage loop are identified: sampling of the output voltage and quantization of the power command signal.

Section 4.2 discusses the effects of output voltage sampling, asynchronously or synchronously with respect to the AC line frequency. Power command quantization and related no limit cycling conditions are presented in Section 6.1. Throughout the chapter, simulation and experimental results are presented for 300W universal input boost PFCs with parameters shown in Figs. 4.1 and 4.2.

4.1 Digital Control of Single-Phase Boost PFC Rectifiers

A brief introduction to the digital average current mode (DACM) PFC is given in Section 2.5.1. The following description expands on the previous introduction and describes the primary DACM PFC's and its variants operating characteristics.

Fig. 4.1 shows a DACM, predictive current control, or equivalent PFC [15–17]. The control

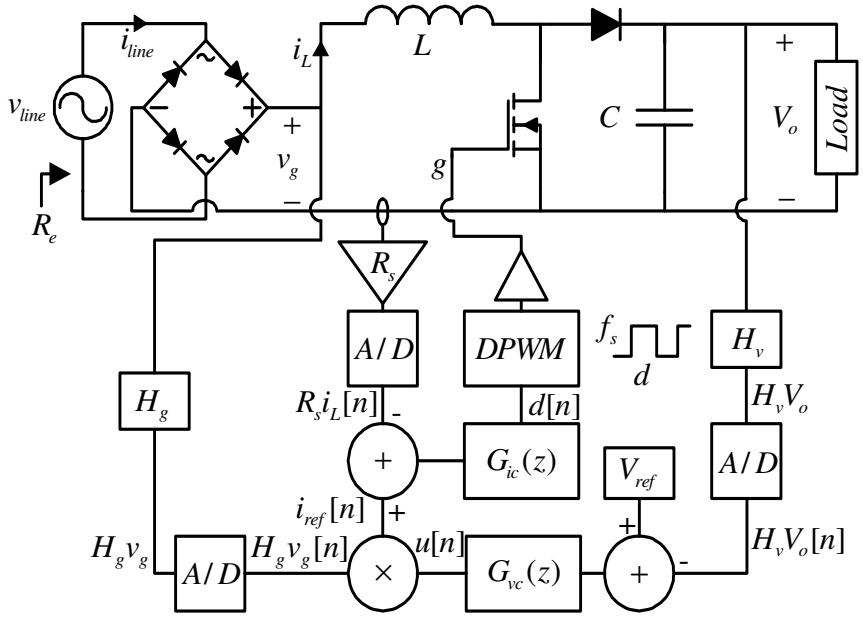


Figure 4.1: DACM controlled PFC boost rectifier, $C = 220\mu$F, $L = 1.5$mH, $H_v = 1/250$, $R_s = 1\Omega$, $V_{o,nominal} = 392$V, $f_s = 68$kHz.

architecture in Fig. 4.1 is a digital implementation of a standard two-loop PFC control architecture [7]. In the current control loop, the boost converter input (inductor) current is sensed and converted to a digital signal i, with an equivalent current-sensing resistance R_s. The sensed current is compared to a reference i_{ref}. The current error is processed by a current-loop compensator (or control law) $G_{ic}(z)$ to produce duty-cycle command $d[n]$ for the digital pulse-width modulator (DPWM). The control objective in the current control loop is to shape the input current to follow the rectified line voltage v_g,

$$\|i_{line}\| = i_L = \frac{v_g}{R_e}\,, \tag{4.1}$$

where R_e is the rectifier emulated resistance. To achieve (4.1), in the DACM PFC of Fig. 4.1, the reference current signal $i_{ref}[n]$ is obtained by sensing the input voltage proportional to v_g, and multiplying this value, $H_g v_g[n]$ with a power command signal $u[n]$. As a result, the emulated resistance in the DACM PFC is

$$R_e = \frac{R_s}{u[n] \times H_g}\,, \tag{4.2}$$

where H_g is the sense network gain for v_g. In the voltage control loop, the output voltage error

is sampled and quantized by an analog-to-digital (A/D) converter. A discrete-time compensator $G_{vc}(z)$ produces the power command signal ($u[n]$) that determines the emulated resistance (R_e) seen by the AC line.

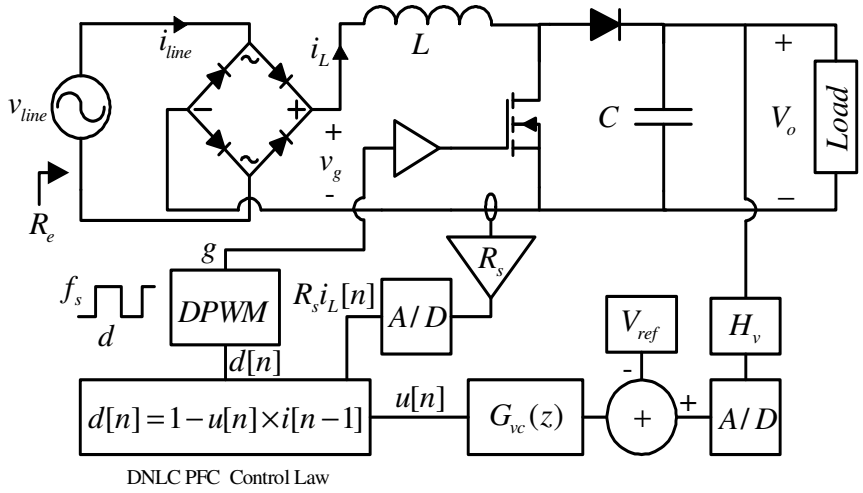


Figure 4.2: DNLC controlled PFC boost rectifier, $C = 220\mu$F, $L = 1.5$mH, $H_v = 1/250$, $R_s = 1\Omega$, $V_{o,nominal} = 392$V, $f_s = 68$kHz.

Fig. 4.2 shows the DNLC PFC controller presented in [51], which is based on the analog nonlinear-carrier (NLC) control approach [14]. In this architecture, the current control loop is considerably simpler. The objective (4.1) is accomplished without the need to sense the input voltage waveform and the current-loop compensator is replaced by a simple current control law shown in Fig. 4.2. In this case, the emulated resistance is [51]:

$$R_e = u[n]V_o R_s \tag{4.3}$$

where V_o is the DC output voltage, and $u[n]$ is again the power command signal.

Assuming ideal operation of the current control loop, the low-frequency large-signal loss free resistor (LFR) model from [7], shown in Fig. 4.3, applies to both the DACM PFC of Fig. 4.1 and the DNLC PFC in Fig. 4.2. This is a low-frequency large-signal model obtained by averaging over a switching cycle under the assumption that the switching frequency f_s is much higher than the AC line frequency f_{line}. The model is commonly used to design the voltage-loop compensator $G_{vc}(z)$.

In following sections, the model of Fig. 4.3 will be used to facilitate the discussion of quantization effects and limit cycle oscillations in the voltage loop.

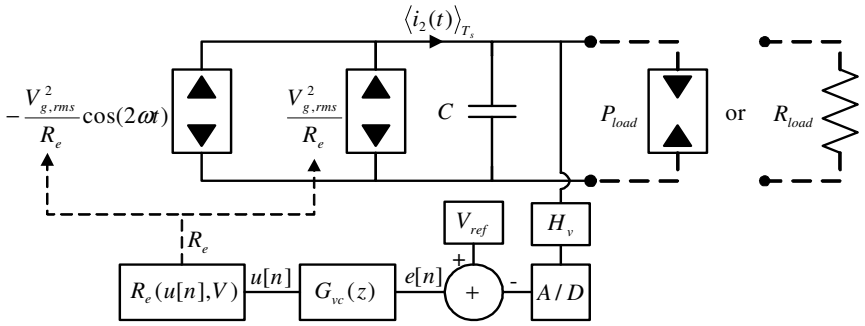


Figure 4.3: Low-frequency large-signal model of an ideal rectifier output port, which appropriately models a PFC operating with a high power factor, and a digital voltage loop.

The power stage model includes a dc power source $V_{g,rms}^2/R_e$ and a time-varying power source at twice the line frequency. Two types of loads are considered: a resistive load (R_{load}) and a constant power-sink load (P_{load}) representative of the case when the PFC is loaded by a downstream DC-DC converter. The emulated resistance R_e is controlled by the power command signal $u[n]$ according to (4.2) for the DACM PFC, or (4.3) for the DNLC PFC. It should be noted that the relationship between the emulated resistance R_e and the power command signal ($u[n]$) is different for the two considered digital PFC control architectures. Section 6.1 discusses how these differences have important implications on limit-cycling in the voltage loops of the two studied PFC architectures.

4.2 Output Voltage Sampling

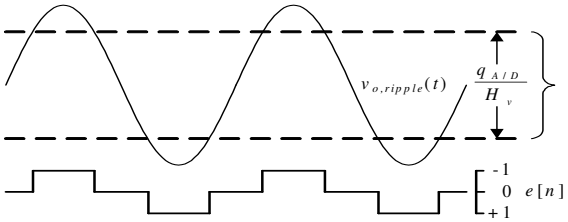
In a digitally controlled PFC the output voltage error is sampled and quantized by a voltage A/D converter. It is assumed that the voltage loop compensator includes integral action in order to achieve zero steady-state error in the DC output voltage V_o. This implies that in normal steady-state operation, the sensed output voltage is expected to be inside the zero-error bin of the voltage A/D converter.

Consider the case when the sampling frequency is equal to the switching frequency (f_s),

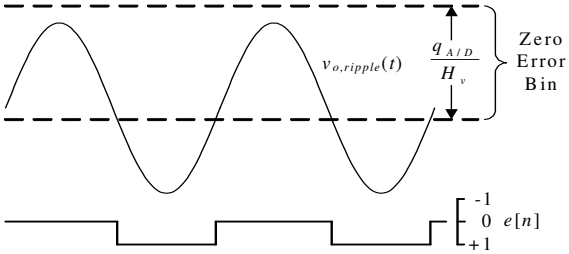
which is significantly higher than twice the ac line frequency ($2f_{line}$) and assume the sampling is nonsynchronous, i.e. the sampling frequency is not an integer multiple of the line frequency. Suppose that the output voltage ripple (at $2f_{line}$) is large enough to overlap into (at least) one error bin on either side of the A/D zero error bin as in Fig. 4.4(a). In this case the dc value of the output voltage is centered in the middle of the zero error bin so it is desirable that this condition result in a constant power command. In order for the integral compensator to make a net zero change over one or more periods of the output voltage ripple it would be necessary to first guarantee that the number of samples that report an error of +1 LSB (least significant bit) equal the number of samples that report an error of -1 LSB. This, however, can be accomplished only if the sampling frequency is an integer multiple of the line frequency. In practice, even if the sampling frequency was an integer multiple of the line frequency, the actual shape of the output voltage ripple could still result in a net error slowly accumulating in the integral compensator, eventually leading to a change in the power command, and resulting in low-frequency limit cycling.

Fig. 4.4(b) shows a situation where the dc value of the output voltage resides in the zero error bin, but over time the integral compensator accumulates error which will result in limit cycling. Widening the zero error bin to include the entire sampled waveform, as in Fig. 4.4(c) is a solution that will result in no limit cycling for nonsynchronous sampling when an integral compensator is used. However, it is difficult to ensure that the size of the zero error bin is wide enough for the entire output voltage ripple waveform given variations in output power and tolerances or variations in the filter capacitance C etc. One possible approach to containing the output voltage ripple in the zero error bin is to adaptively adjust the size of the zero error bin [17]. Using this approach, the output voltage can be sampled at a high rate which is particularly advantageous in the design of a fast voltage control loop as discussed in [17, 55].

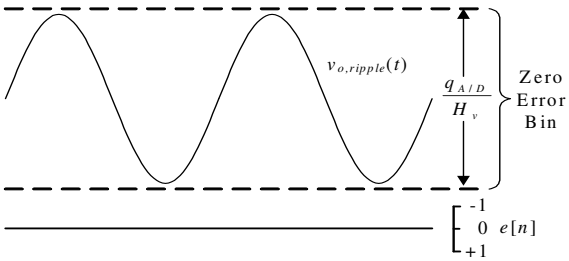
More conventionally, synchronizing the sampling of the output voltage at $2f_{line}$ (or f_{line}) provides a sampling method that can avoid limit cycling in the power command as shown in Fig. 4.4(d). Similar to sampling at the switching frequency in a DC-DC converter to avoid varied sampled values due to switched waveform ripples, sampling at the frequency of the output voltage



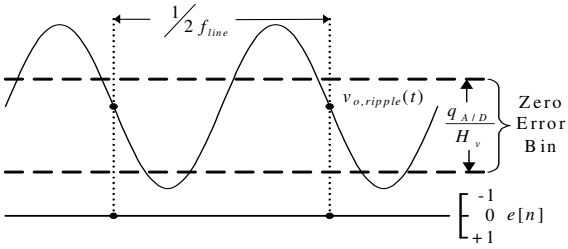
(a) Fast nonsync. sampling example I.



(b) Fast nonsync. sampling example II.



(c) Widening of the zero error bin to achieve zero error in steady state.



(d) Synchronous sampling at $2f_{line}$ to achieve zero error in steady state.

Figure 4.4: Examples of waveforms that lead to non zero error in steady state and illustrations of two methods to achieve zero steady state error.

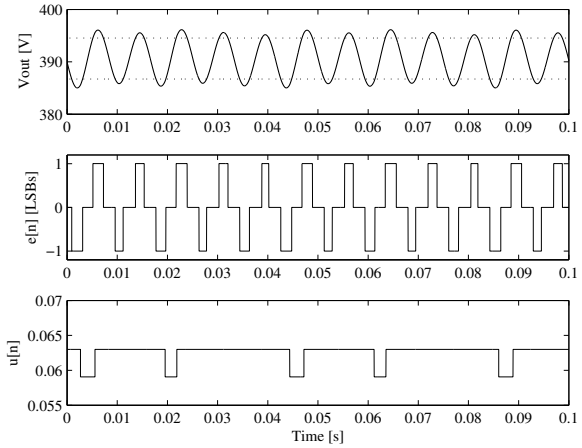
ripple effectively reduces the steady state value of the output voltage to a dc value as seen by the discrete-time compensator. Note that due to the significant output voltage ripple the effective DC output voltage sensed by the output voltage A/D depends on when the samples are taken. In practice, sampling the output voltage around the input voltage or current zero crossings provides output voltage samples near the actual dc output voltage values.

Synchronizing the outer voltage loop to the line frequency can be accomplished using phase-locked loop techniques, but much simpler approaches are also feasible. For example, in the DACM PFC controller the line voltage sense can be used to trigger voltage samples and generate the voltage control loop clock using a digital comparator with hysteresis. The same technique can be used in the DNLC PFC controller using either the duty cycle command or the inductor current samples directly since an input voltage waveform is not necessarily sensed. Both controllers require that a minimum sampling frequency be maintained for voltage loop operation during startup. This is accomplished using a low frequency clock and a counter. The minimum voltage loop clocking frequency should be set below the lowest expected normal operating frequency. A value of 80Hz ($2f_{min}$) was used in the experimental prototypes allowing normal synchronous sampling operation at both 50 and 60Hz line frequencies.

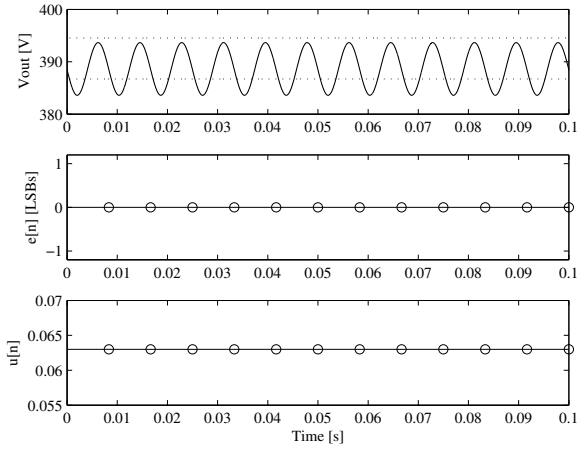
Nonsynchronous and synchronous sampling methods were simulated by implementing the model shown in Fig. 4.3 using Simulink®. Fig. 4.5 shows the output voltage including the ac ripple (V_o), the sampled output voltage error ($e[n]$) and the power command ($u[n]$) for the operation of DNLC PFC controller with fast nonsynchronous (Fig. 4.5(a)) and synchronous (Fig. 4.5(b)) sampling methods. In both cases, the no limit cycling conditions related to the power command quantization discussed in Section 6.1 are met. The waveform in Fig.4.5(a) is similar to the type of limit cycling described in Fig. 4.4(a) and, as expected, a low frequency limit cycle is produced even though the DC value of the output voltage never leaves the zero error bin. Note that the dc output voltage is well centered in the zero error bin due to the limit cycling oscillations resulting in an effect similar to eliminating the zero error bin altogether as in [56].

When synchronous sampling is implemented as in Fig. 4.5(b), the controller is unaffected by

the output voltage ripple at $2f_{line}$ and limit cycling of the power command signal is avoided.



(a) Nonsynchronous sampling at f_s=68kHz leading to limit cycling, voltage loop controller $BW \approx .5$Hz.



(b) Synchronous sampling at $2f_{line}$, sampling instances shown by $\circ$, voltage loop controller $BW \approx$ 10Hz.

Figure 4.5: Nonsynchronous and synchronous sampling instances using the DNLC PFC controller, $P = 300$W, $V_{g,rms} = 85V$, with a resistive load, dashed lines show the bounds of the zero error bin.

4.3 Power Command Quantization

This section discusses the effects of power command (u) quantization given that synchronous sampling or an adaptively adjustable zero error bin are implemented to avoid low-frequency limit cycling induced by sampling of the output voltage. Power command quantization in a PFC rec-

tifier is similar in nature to the duty cycle command quantization in digitally controlled DC-DC converters analyzed by [53, 54]. Following a similar analysis, a static no limit cycling condition can be expressed as:

$$G_{vu0} H_v q_u < q_{A/D}\,, \tag{4.4}$$

where q_u and $q_{A/D}$ are the LSB values of the power command signal u and the output voltage sense respectively. G_{vu0} is the low-frequency small-signal gain from the power command u, to the output voltage V_o.

Condition (4.4) relates the resolutions of the power command signal and the A/D resolution used for output voltage sensing. It implies that there exists a value of u that results in an output voltage that resides in the zero error bin.

To reach a steady state after a transient, the integral action of the compensator must step through the values of $u[n]$ in such a way that the zero error bin is not skipped over. Similar to the analysis presented in [54], this leads to another no limit cycling condition,

$$G_{vu0} H_v K_i < 1\,, \tag{4.5}$$

where K_i is the integral gain of the voltage loop compensator. Condition (4.5) guarantees that the solution(s) in the zero error bin provided by (4.4) can be resolved by the digital controller following a transient. The integral gain term of a proportional-integral (PI) discrete-time compensator typically employed in the slow outer voltage loop can be determined by expanding the compensator as:

$$G_{vc}(z) = \frac{u(z)}{e(z)} = K\frac{(z-\alpha)}{(z-1)} = K_p + K_i\frac{z}{(z-1)}\,, \tag{4.6}$$

resulting in

$$K_i = K(1-\alpha)\,, \tag{4.7}$$

which can then be used in (4.5).

In practice, the limit cycling conditions (4.4) and (4.5) both need to be satisfied by a margin dependent on the amount of sampling noise, converter efficiency etc. It is important to note that

both conditions depend on the low frequency gain G_{vu0} of the control to output transfer function. This gain can be determined by small-signal linearization of the large-signal averaged model shown in Fig. 4.3. Following the approach in [7], first the LFR output port model is averaged over one half of the input line period to remove the time varying power term. The resulting model remains valid for frequencies considerably lower than twice the input line frequency. This simplified model, whose average output current is defined as

$$\langle i_2(t)\rangle_{T_{2L}} = \frac{\langle p(t)\rangle_{T_{2L}}}{\langle v_o(t)\rangle_{T_{2L}}} = \frac{v_{g,rms}^2(t)}{R_e(u(t), v_o(t))\langle v_o(t)\rangle_{T_{2L}}} \tag{4.8}$$

is then perturbed and linearized using a three-dimensional Taylor expansion about a quiescent operating point. This results in the small signal model shown in Fig. 4.6 [7], where:

$$-\frac{1}{r_2} = \left.\frac{d\langle i_2(t)\rangle_{T_{2L}}}{d\langle v_o\rangle_{T_{2L}}}\right|_{\langle v_o\rangle_{T_{2L}}=V_o} \tag{4.9}$$

and

$$j_2 = \left.\frac{d\langle i_2(t)\rangle_{T_{2L}}}{du}\right|_{u=U} \tag{4.10}$$

The g_2 term in the model is omitted from calculations here as $\hat{v}_{g,rms}$ equals zero when determining $G_{vu}(s)$. For the DNLC PFC controller, the emulated resistance is found from (4.3). The model

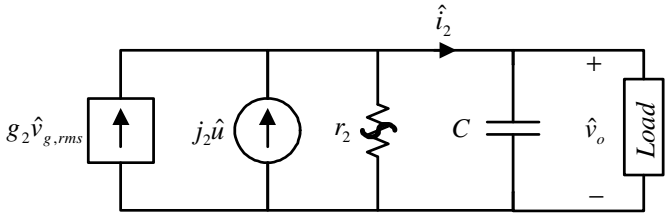


Figure 4.6: Small-signal model of the PFC rectifier.

averaged over one half the line period results in

$$\langle i_2(t)\rangle_{T_{2L}} = \frac{v_{g,rms}^2(t)}{u\langle v_o(t)\rangle_{T_{2L}}^2 R_s} \tag{4.11}$$

Taylor expansion of the above produces

$$-\frac{1}{r_2} = -\frac{2V_{g,rms}^2}{UV_o^3R_s} = -\frac{2P}{V_o^2} = -\frac{2}{R} \tag{4.12}$$

and

$$j_2 = \frac{V_{g,rms}^2}{U^2 V_o^2 R_s} = -\frac{P^2 R_s}{V_{g,rms}^2} \tag{4.13}$$

Solving the model in Fig. 4.6, also from [7], for the control to output transfer function assuming a resistive load yields

$$G_{vu}(s) = \left.\frac{\hat{v}_o}{\hat{u}}\right|_{\hat{v}_{g,rms}=0} = -\frac{PV_o^2 R_s}{3V_{g,rms}^2}\left(\frac{1}{1+sCR/3}\right) \tag{4.14}$$

Table 4.3 lists the above result and other control-to-output transfer functions for the DNLC and DACM PFCs for both resistive and constant power loads.

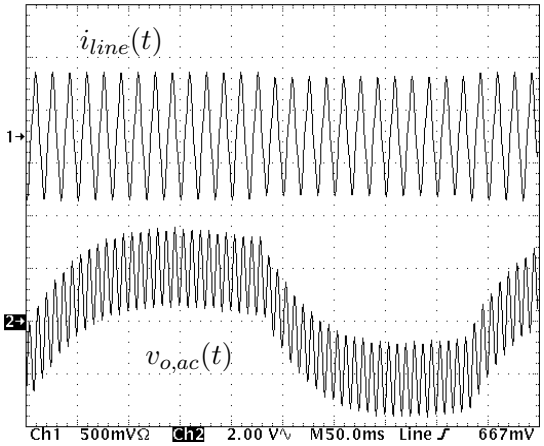
Table 4.1: Derived control to output transfer functions for the DNLC and DACM PFC controllers.

	DNLC Controller	DACM Controller
Load	$G_{vu}(s) = \frac{\hat{v_o}(s)}{\hat{u}(s)}$	$G_{vu}(s) = \frac{\hat{v_o}(s)}{\hat{u}(s)}$
R_{load}	$\frac{-PV_o^2 R_s}{3V_{g,rms}^2}\left(\frac{1}{1+sCR/3}\right)$	$\frac{V_o V_{g,rms}^2 H_g}{2PR_s}\left(\frac{1}{1+sCR/2}\right)$
P_{load}	$\frac{-PV_o^2 R_s}{V_{g,rms}^2}\left(\frac{1}{1+sCR}\right)$	$\frac{V_{g,rms}^2 H_g}{sV_o C R_s}$

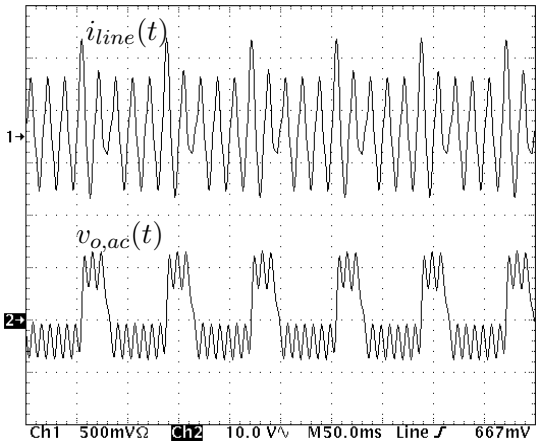
4.3.1 Voltage Loop Limit Cycling in PFC Rectifiers with Digital Average Current Mode Control

For the case of the DACM PFC with a resistive load the maximum dc gain occurs at minimum power and maximum input voltage. The experimental DACM PFC of Fig. 4.1 was tested at an input voltage of 220V$_{rms}$ and an output power of 75W (this point was chosen because it represents a point where the control to output transfer function of the DACM PFC is large for the resistive load case and the current control loop gave satisfactory performance to insure high power factor operation). Fig. 4.7 waveforms show limit cycling due to violation of (4.4) (Fig. 4.7(a)), limit cycling due to violation of (4.5) (Fig. 4.7(b)), and no limit cycling when both conditions are satisfied (Fig. 4.7(c)). In all cases, the power command signal u is represented by 13-bits ($q_u = 1/2^{13}$) and $H_g \approx 1$ as v_g is divided by 250 before the A/D but digitally multiplied by 256 before multiplication with u. The controller implemented to produce the waveforms in Fig. 4.7(a) utilizes a 6-bit output voltage

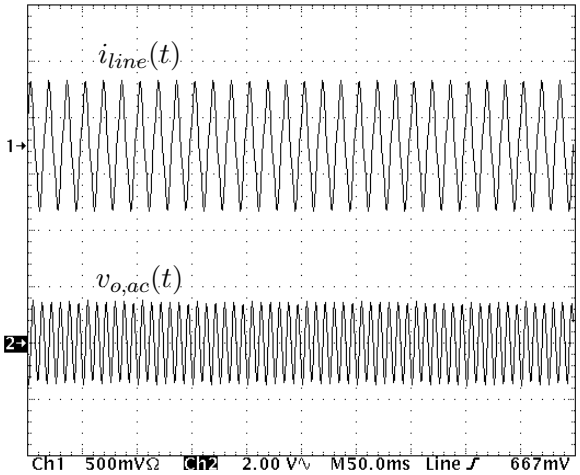
ADC ($q_{A/D}/H_v = 7.8V$) and a low K_i compensator so that (4.5) is satisfied. Fig. 4.7(b) shows the waveforms of the DACM PFC when the output voltage A/D resolution has been reduced to 5-bits and the compensator integral gain is set at 0.03125, violating (4.5). This figure also shows how a dc current component could be drawn from the ac line if the limit cycle oscillations between power settings occurred synchronously with the line frequency. When the compensator integral gain is reduced to 0.00098, satisfying (4.5), no limit cycling is observed as shown in Fig. 4.7(c).



(a) DACM PFC waveforms exhibiting limit cycling due to improper specification of q_u and $q_{A/D}$ for resistive load operation, violating (4.4).



(b) DACM PFC waveforms exhibiting limit cycling due to excessive K_i for a resistive load operation, violating (4.5).



(c) DACM PFC waveforms showing operation with no limit cycling with a resistive load, both (4.4) and (4.5) are satisfied.

Figure 4.7: Experimental steady state waveforms collected using a DACM PFC controller with synchronous sampling at $2f_{line}$ and a resistive load, $P = 75$W, $V_{g,rms}= 220$V.

For the case of a constant power load, notice that the DACM PFC controller has an infinite DC gain (G_{vu0}) which implies, by either (4.4) or (4.5), that avoiding limit cycling in such a converter is not possible. If the power taken by the load does not exactly match one of the possible power processing points, set by quantized u, the voltage across the output capacitor will either increase or decrease until it leaves the zero error bin requiring corrective action by the voltage loop resulting in limit cycling. Fig. 4.8 shows the results of operating the same DACM PFC controller as in Fig. 4.7(c) but with a constant power load of 300W. Low frequency limit cycling is apparent as the output voltage of the PFC stage continuously increases or decreases until it reaches the limits of the zero error bin and the voltage control loop changes the power command signal. Such limit cycling may occur at very low frequency, and may not be easily noted or present a problem in practice. Nevertheless, the fact that the DACM PFC with power sink load is bound to exhibit limit cycling oscillations is worth noting since this is a common situation in practice when the load is a tightly regulated high-efficiency DC-DC converter. The effects of low-frequency limit-cycling leading to undesirable dc or even harmonics and flicker in the ac line current should be considered.

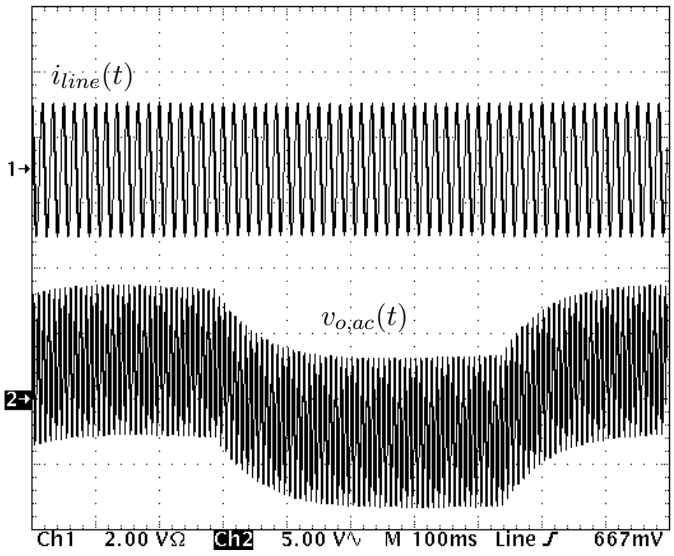


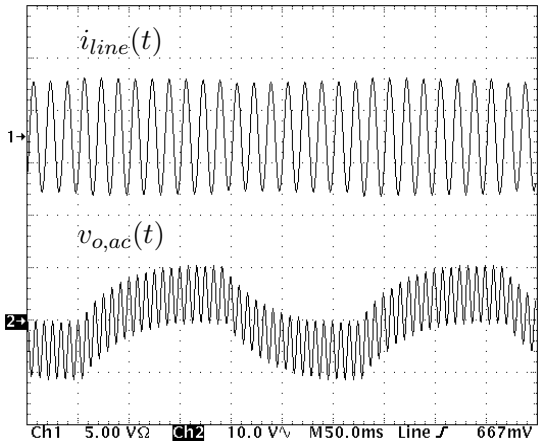
Figure 4.8: Experimental waveform, showing low frequency limit cycling, collected using the DACM PFC controller with synchronous sampling at $2f_{line}$ and a constant power load, $P = 300$W, $V_{g,rms}=$ 220V.

4.3.2 Voltage Loop Limit Cycling in PFC Rectifiers with Digital NLC Control

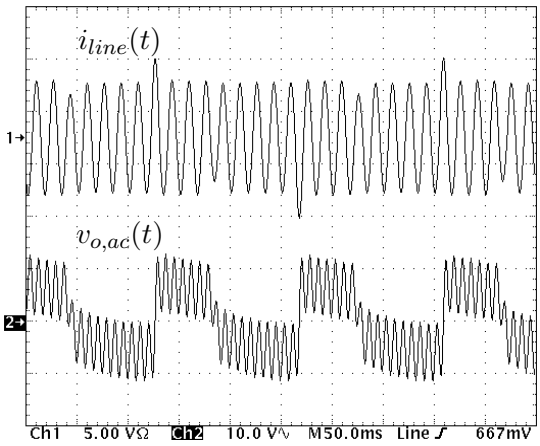
In contrast to the DACM PFC, the maximum DC gain for the DNLC PFC occurs at maximum power and minimum input voltage. Furthermore, for the case of constant power load, the dc gain is three times larger, but not infinite as is the case in DACM PFC. As shown by (4.3), the emulated input resistance for the DNLC PFC is a function of the quantized power command signal and the DC output voltage V_o. There exists a negative feedback between the output voltage and the input power for the DNLC PFC guaranteeing that the no limit cycling conditions (4.4) and (4.5) can be met even in the case of constant power load. With reference to (4.3), suppose that u is set to a quantized value that causes the PFC stage to produce slightly more power than the load draws from the output. The output voltage will begin to increase which in turn results in an increase of the emulated resistance (R_e) as u remains constant. The increase in R_e reduces the power input to the PFC stage reducing the amount of power provided to the output which slows the rise of the output voltage due to the power imbalance between the PFC and the load. This process continues until the input power exactly matches the output power plus any losses in the PFC stage. As long as the output voltage remains in the zero error bin no adjustment of the power command signal is necessary, which means that steady-state operation without limit cycling is realizable.

As the dc control to output gains of the DNLC PFC are identical for the cases of resistive and constant power load, except for a factor of three, the results of testing the experimental DNLC PFC of Fig. 4.2 are shown only for the case of the constant power load, the more stringent of the two cases. The converter was tested at the expected worst case point for limit cycling, $P = 300$W and $V_{g,rms} = 85$V. Fig. 4.9(a) shows the waveforms collected when u is represented by 9-bits ($q_u = 1/2^9$). The output voltage was sensed with a 6-bit A/D resulting in a $q_{A/D}/H_v$ of $7.8V$. The compensator used had a low integral gain so as to not violate (4.5). The output voltage A/D resolution was reduced to 5-bits ($q_{A/D}/H_v = 15.6V$) and the compensator was modified to give an integral gain of $K_i = 0.0625$ to produce the PFC waveforms shown in Fig. 4.9(b). As expected from (4.5) limit cycling due to excessive integral gain is observed. Fig. 4.9(c) shows the PFC waveforms

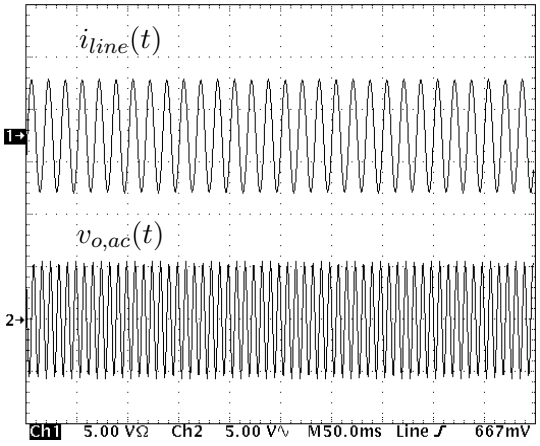
when the voltage loop controller is designed to avoid limit cycling. The power command signal is represented by 9-bits, the output voltage is sensed using 5-bits and the integral gain of the controller is 0.03125, meeting both conditions (4.4) and (4.5).



(a) DNLC PFC waveforms exhibiting limit cycling due to improper specification of q_u and $q_{A/D}$ for constant power load operation, violating (4.4).



(b) DNLC PFC waveforms exhibiting limit cycling due to excessive integral gain for constant power load operation, violating (4.5).



(c) DNLC PFC waveforms showing operation with no limit cycling with a constant power load, both (4.4) and (4.5) are satisfied.

Figure 4.9: Experimental steady state waveforms collected using the DNLC PFC controller with synchronous sampling at $2f_{line}$ and a constant power load, $P = 300$W, $V_{g,rms}$= 85V.

Finally, it is worth noting that the demand for the relatively high-resolution power command signal u, in a digitally controlled PFC rectifier is not difficult to meet. In contrast to difficulties

related to the demand for a high-resolution DPWM in DC-DC converters, where the resolution is limited by the hardware speed, a high-resolution u simply requires sufficiently long registers. In addition, hardware requirements can be reduced further by employing $\Sigma\Delta$ modulation techniques as shown in Section 3.2.3.

4.4 Chapter Summary

This chapter examines quantization effects and limit cycling in the voltage control loop of DACM and DNLC controlled single-phase power factor correction (PFC) rectifiers. Low-frequency limit cycling in the voltage loop can result in highly undesirable DC components, even harmonics in the AC line current and flicker. It is shown that two mechanisms can result in low-frequency limit-cycling: nonsynchronous sampling of the output voltage and quantization of the power command signal. Simulations confirm the benefit of sampling the output voltage synchronously at $2f_{line}$. Experiments confirm the validity of the two presented no limit cycling conditions. It is further demonstrated that limit cycling is unavoidable in the case of the DACM PFC when loaded with a constant power load whereas the DNLC PFC allows for no limit cycling operation under the same load conditions.

Chapter 5

Single Comparator A/D Converter for Output Voltage Sensing of Single Phase PFC Rectifiers

Many implementations of digital voltage loops for use in power factor correction (PFC) rectifiers have been proposed to either improve the dynamic response to line and load transients [9,15,17,26] or reduce the hardware complexity of a complete PFC controller [25,27]. In all cases the scaled output voltage ($H_v V_o$) or the scaled error voltage ($H_v V_e$) of the PFC stage was sampled using a medium resolution (8-10 bit) analog to digital converter (A/D). A new method for determining the digital value of the output voltage error signal using only a single analog comparator and a small amount of digital hardware is proposed in this chapter. Throughout this thesis this method is referred to as the single comparator A/D (SCA/D).

In fully digital PFC's such as in [15, 17, 51], the inductor or switch current is sampled as described in Chapter 2 which typically requires a relatively fast A/D as sampling typically occurs at the converter switching frequency (f_s). This A/D is usually easily multiplexed to also measure the output voltage of the PFC rectifier. However, in hybrid architectures PFC's such as [24–27], where the current loop is closed using analog control techniques and the voltage loop is implemented digitally, the proposed technique eliminates the need for a traditional A/D altogether. Additionally, the proposed output voltage sampling technique retains the desirable qualities of a typical digital voltage loop such as the ability to implement a fast voltage loop. Also, the proposed voltage loop inherently samples the output voltage synchronously at twice the line frequency ($2f_{line}$) which results in a reduced hardware implementation digital voltage loop compensator compared to sampling

at the PFC converter switching frequency (f_s), allows for the avoidance of power command limit cycling as described in Chapter 3, and decreases input current total harmonic distortion (THD) by completely rejecting the output voltage ripple from the power command signal. The complete rejection of the twice the line frequency ($2f_{line}$) ripple component on the output voltage is accomplished by synchronously sampling the output voltage at $2f_{line}$and not by previously reported methods such as filtering of the output voltage sense signal [15,16], placing the entire voltage ripple in the zero error bin of the voltage sensing A/D [17] or the implementation of a sinusoidal reference based on the estimation of the output capacitance and the measurement of the operating power [9].

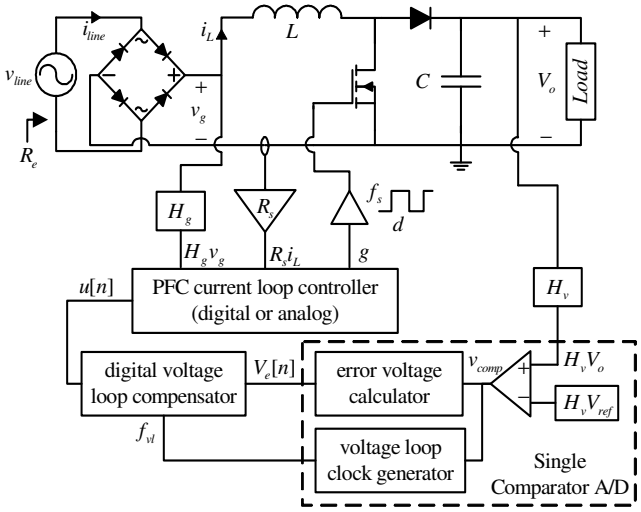


Figure 5.1: Boost PFC stage with single comparator A/D.

Fig. 5.1 shows a boost PFC stage with the proposed SCA/D and a digital voltage loop. The SCA/D is made up of three parts including the analog comparator with voltage reference, the error voltage calculator and the voltage loop clock generator. The power stage specifications are given in Table 5.1. The current loop may be of any control type such as average current mode (ACM) [15–17] or nonlinear carrier (NLC) [12,14,32,51,57] control. Furthermore, the current control loop may be implemented in a digital or analog design space. When the SCA/D is paired with an NLC type current controller an inherent power feedforward gain compensation of the voltage loop is achieved effectively reducing the outer voltage loop gain variation as power processing levels of the PFC

stage change.

Table 5.1: SCA/D PFC stage parameters.

Parameter	Value
C	100μF
L	1.5mH
$V_{o,nominal}$	385V
f_s	65kHz
H_v	1/250
$P_{o,max}$	300W

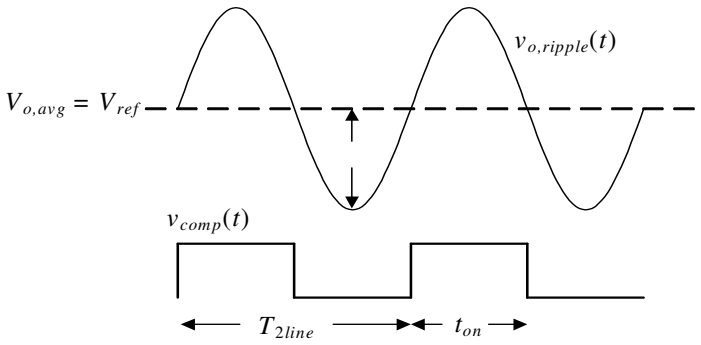
Section 5.1 describes the operation, implementation and characteristics of the SCA/D. The power feedforward feature of the SCA/D is discussed in Section 5.2. Experimental results including waveforms of steady-state operation and verification of improved load transient response when the SCA/D is utilized to give a power feedforward gain are presented in Section 5.3. Section 5.3 also includes a discussion on the operation of the SCA/D when saturated and output voltage load transient responses are shown for such operation.

5.1 Single-Comparator A/D (SCA/D) Operation

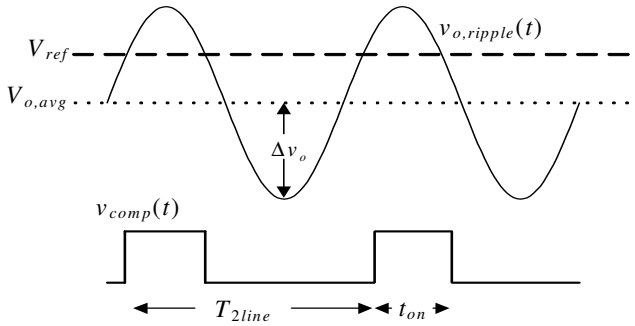
The basic operational concept of the SCA/D is described in Section 5.1.1 below. Section 5.1.2 follows and mathematically relates the output of the single analog output voltage sensing comparator to the average PFC dc output voltage. Along with a single analog comparator the SCA/D requires two digital blocks. These two digital logic blocks are described in detail in Sections 5.1.3 and 5.1.4. Section 5.1.5 presents the specific hardware configuration and requirements used in the SCA/D prototype. The describing function and and the effects of SCA/D saturation are discussed is Section 5.1.6.

5.1.1 SCA/D Concept

Referring to Fig. 5.1, the output voltage (V_o), which has a significant ac ripple component due to the inherent instantaneous power imbalance between the PFC input and output over a



(a) SCA/D conceptual waveforms when $V_{o,avg} = V_{ref}$.



(b) SCA/D conceptual waveforms when $V_{o,avg} < V_{ref}$.

Figure 5.2: SCA/D example waveforms.

half line cycle, is first scaled by a divider network (H_v) and then connected to a single analog comparator. The other comparator input is connected to a constant reference signal (V_{ref}) which sets the regulated output voltage set point ($V_o = V_{ref}/H_v$). Fig. 5.2(a) shows conceptual waveforms for the ac output voltage ripple and the comparator output (v_{comp}) waveform when the converter operates at or near regulation. As shown the waveform at the output of the comparator (v_{comp}) will be a square wave with a frequency of $2f_{line}$ and a duty cycle ($d_{comp} = t_{on}/T_s$) of 50%. Fig. 5.2(b) shows the SCA/D conceptual waveforms when the average output voltage is slightly lower than the designed reference voltage. In this case the output voltage ripple is not centered around the reference voltage so the resulting v_{comp} waveform shows a duty cycle less than 50%. If the average output voltage were higher than V_{ref} the duty cycle of the v_{comp} waveform would be higher than 50%. By regulating the duty cycle of v_{comp} to be equal to 50% via the power command output ($u[n]$) of the voltage loop compensator the output voltage will be regulated to V_{ref}/H_v.

The output error voltage (V_e) is determined by the error voltage calculator block shown in Fig. 5.1 that consists of the required digital hardware to determine the duty cycle of the incoming v_{comp} signal over a period of $1/(2f_{line})$ and relates the acquired duty cycle to a specific error voltage. The error voltage signal is then utilized by the digital voltage loop compensator which outputs the power command signal $u[n]$. The power command signal determines the amount of power being processed by the PFC stage and is adjusted by the voltage loop compensator to regulate the output voltage of the PFC rectifier. The voltage loop clock generator produces a clock (f_{vl}) that is synchronous to f_{line} and has a nominal frequency of $2f_{line}$.

5.1.2 Relationship Between d_{comp} and V_e

Inspection of Figs. 5.2(a) and 5.2(b) it is apparent that the SCA/D will only provide an accurate voltage measurement when the output voltage ripple crosses the reference voltage set point twice during a half line period. This reduces the sensing output voltage range to the peak-to-peak ac ripple voltage ($2\Delta v_o$). In effect, the proposed SCA/D creates a windowed sample of the output voltage centered around the steady state regulation point with a window range of $\pm\Delta v_o$. One half of the peak-to-peak output voltage ripple can be found approximately as [7]:

$$\Delta v_o \approx \frac{P}{4\pi f_{line} C V_{o,rms}} \tag{5.1}$$

The ideal relation between d_{comp} and V_e is found as:

$$V_e = \Delta v_o \sin((d_{comp} - 0.5)\pi) \tag{5.2}$$

assuming that the output voltage ripple can be approximated as sinusoidal. This assumption is quite accurate as long as the PFC stage is capable of low THD rectification. As shown in (5.1), Δv_o is proportional to the operating power of the PFC stage (P) and inversely proportional to the line frequency (f_{line}), the output capacitance value (C) and the rms output voltage ($V_{o,rms}$). Directly calculating V_e using (5.2) would require that these previously mentioned variables, P, C, f_{line}, be available for the computation of Δv_o. While f_{line} and $V_{o,rms}$ are bounded in typical applications

the remaining variables, which can be thought of in terms of μF/W, vary greatly depending on the power processing level of the stage during a particular operating period. No attempt has been made to determine Δv_o in (5.2) according to operating conditions so that the calculated V_e accurately represents the actual error voltage at any particular operating point other than during regulation (i.e. $V_e = 0$). In fact, attempting to scale Δv_o with operating conditions would eliminate the power feedforward mechanism described in Section 5.2. Furthermore, the digital calculation of a sine relation, as in (5.2), typically requires a look-up-table (LUT) resulting in a relatively large amount of digital hardware required for the digital implementation. A simplified linear approximation of (5.2) with Δv_o replaced by a constant scalar (V_K) was investigated with the aim of simplifying the digital hardware implementation. This linear relationship between the single comparator duty cycle and the error voltage is described by:

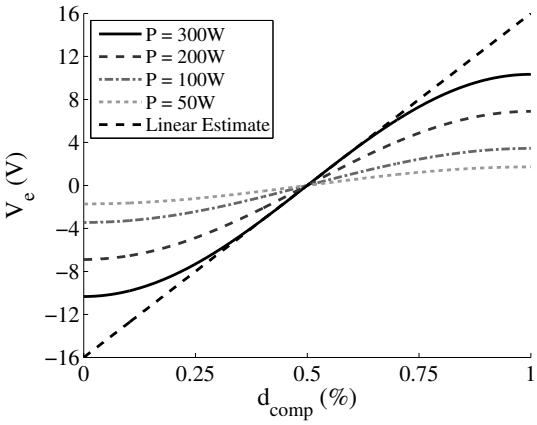
$$V_e[n] = V_K(2d_{comp}[n] - 1) \tag{5.3}$$

This linearized relation was determined by simply making the relation between $d_{comp}[n]$ and $V_e[n]$ purely linear over the ranges of $d_{comp}[n] = 0 \rightarrow 1$ and $\pm V_K$ respectively. The magnitude of V_K sets the gain of the SCA/D and was chosen so that the gain of the linear estimation (5.3) approximately matched the gain of the ideal SCA/D around regulation during full power operation (see Sec. 5.2 for details) at a line frequency of 60Hz. This constant is found by

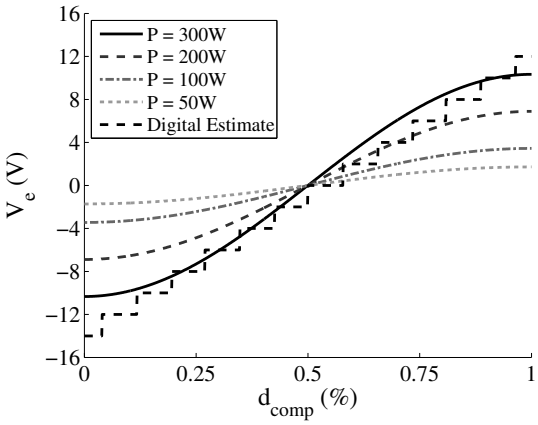
$$V_K = \frac{P_{max}}{8 f_{line} C V_{o,rms}} \tag{5.4}$$

Computing (5.4) for the PFC stage specifications given in Table 5.1 and $f_{line} = 60$Hz results in $V_K \approx 16$V.

Fig. 5.3(a) shows the ideal relationship between d_{comp} and V_e for various power levels as well as the approximate linear relationship given by (5.3) with $V_K = 16$V for the power stage shown in Fig. 5.1 and a line frequency of 60Hz. As can be determined from the figure the error in measuring V_e can be quite large especially when the converter operates at lower power levels and the error voltage (V_e) is not near zero. However, around regulation ($d_{comp} = 0.5, V_e = 0$) the

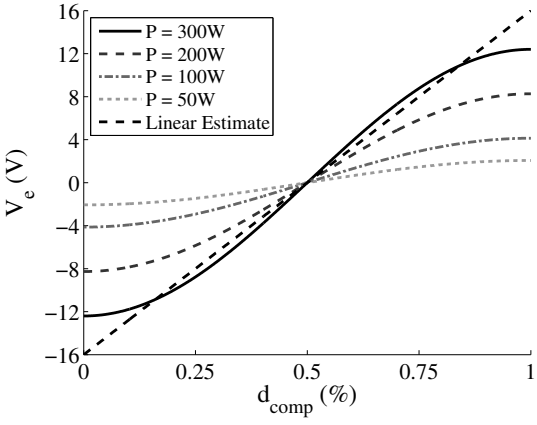


(a) Relation between d_{comp} and V_e and the linear relation given by (5.3), $f_{line} = 60$Hz.

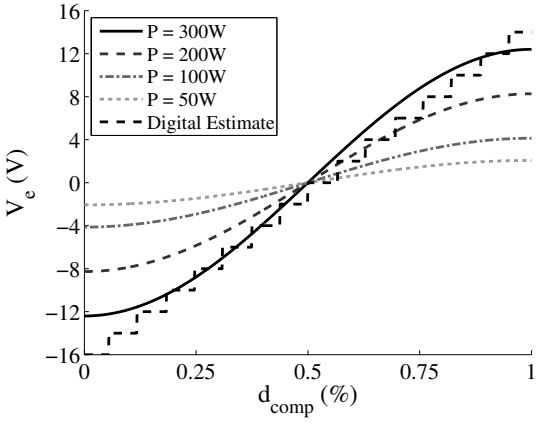


(b) Relation between d_{comp} and V_e and the implemented digital relation showing quantization, $f_{line} = 60$Hz.

Figure 5.3: Relations between d_{comp} and V_e, $f_{line} = 60$Hz.



(a) Relation between d_{comp} and V_e and the linear relation given by (5.3), $f_{line} = 50$Hz.



(b) Relation between d_{comp} and V_e and the implemented digital relation showing quantization, $f_{line} = 50$Hz.

Figure 5.4: Relations between d_{comp} and V_e, $f_{line} = 50$Hz.

linearly approximated SCA/D given by (5.3) reports an error voltage of zero regardless of the power processing level of the PFC stage. Also, with V_K chosen according to (5.4), it is apparent that the gain (slope) of the linearly approximated SCA/D matches the gain of the ideal SCA/D around regulation at full rated power. Fig. 5.4(a) shows the ideal relationship between d_{comp} and V_e as in Fig. 5.3(a) but for a line frequency of 50Hz. The subtle differences between the ideal relations at 50Hz operation and 60Hz operation are due to slightly increased output voltage ripple magnitudes when operating at the lower line frequency. The increased ripple is described by

$$\Delta v_{o,1} = \frac{f_{line,2}}{f_{line,1}} \Delta v_{o,2} \tag{5.5}$$

where $\Delta v_{o,1}$ and $\Delta v_{o,2}$ are the peak-to-peak output voltage ripples at line frequencies of $f_{line,1}$ and $f_{line,2}$ respectively.

5.1.3 Calculating the Error Voltage

Fig. 5.5 shows the internal components of the SCA/D. Referring to the error voltage calculator block, two n-bit counters are used to measure the effective on-time (t_{on}) and off-time (t_{off}) of the v_{comp} signal. Both counters are reset on the rising edge of f_{vl} delayed by $1/f_{sys}$. The registers then increment depending on the state of v_{comp}. The t_{on} register increments when v_{comp} is one and the t_{off} register increments when v_{comp} is zero. Two comparators monitoring the t_{on} and t_{off} registers trigger the voltage loop clock, f_{vl} if either register contains a value higher than $t_{overflow}$. The comparators outputs, $t_{on,of}$ and $t_{off,of}$, are inputs to the voltage loop clock generator and are used to maintain minimum voltage loop clocking during SCA/D saturation.

In order to minimize regulation offset errors and simplify the hardware implementation of the SCA/D, (5.3) is rewritten as:

$$V_e[n] = V_K \left(\frac{t_{on}}{T} - \frac{t_{off}}{T} \right) \tag{5.6}$$

where

$$T = t_{on} + t_{off} = \frac{1}{2 f_{line}} \tag{5.7}$$

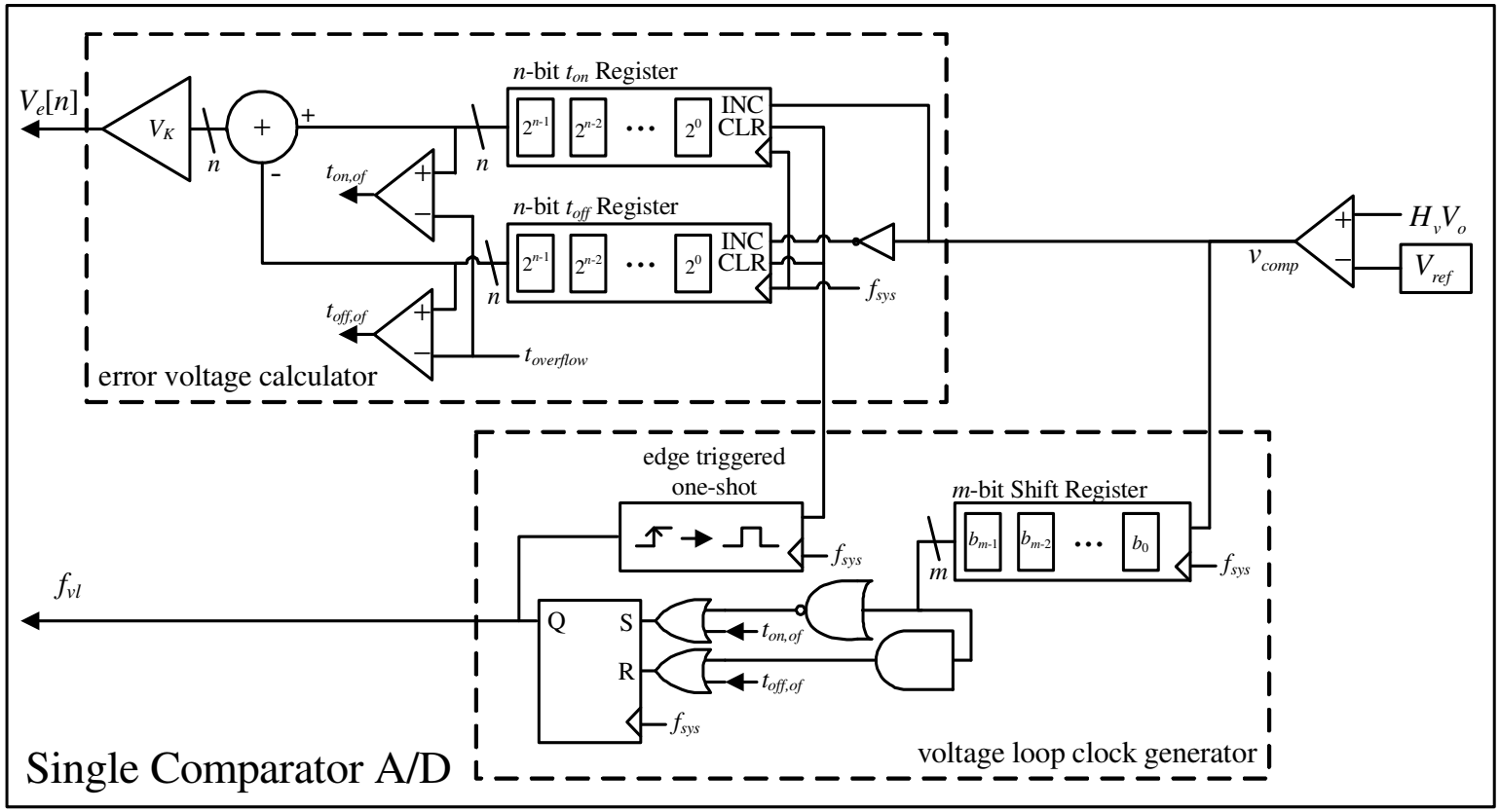


Figure 5.5: Schematic of the SCA/D including: single analog comparator, error voltage calculator block, and voltage loop clock generator.

Multiplication of (5.6) by T/T_{max} where $T_{max} = f_{sys}2^n$ and n is the counter length results in the following relation that is easier to evaluate using digital hardware,

$$V_e[n] = \frac{T}{T_{max}} V_K \left(\frac{t_{on}}{T_{max}} - \frac{t_{off}}{T_{max}} \right) \tag{5.8}$$

where the raw count values of the t_{on} and t_{off} registers are exactly equal to the ratios t_{on}/T_{max} and t_{off}/T_{max}. Obviously V_K is now scaled by a line-frequency dependent scalar (T/T_{max}) that lowers the effective magnitude of the possible error voltage reported as $T_{max} > T$. This scalar is equal to 0.80 and 0.96 for line frequencies of 60 and 50Hz respectively for the implemented system. A digital phase locked loop (DPLL) could be implemented to produce a digital clock that had 2^n clock periods per half line cycle regardless of line frequency. This clocking arrangement would eliminate the above described line frequency gain dependency. Such a system was not implemented as the added line frequency dependent scalar did not greatly effect the performance of the outer voltage loop with an implemented SCA/D.

Fig. 5.3(b) shows the ideal SCA/D relation between d_{comp} and the digitally implemented relation as given by (5.8) for f_{line} = 60Hz and an ideal 2V quantization level of $V_e[n]$ at rated power. Due to the frequency dependent scalar the maximum range of the reported error voltage is -14V to 12V. Also, one can see that any v_{comp} duty cycle between 0.5 and about 0.6 will result in zero reported error. This is the zero error bin in terms of d_{comp}. Fig. 5.4(b) shows the implemented digital SCA/D relation for f_{line} = 50Hz. The output range of the SCA/D is -16V to 14V under these operating conditions.

5.1.4 Generation of f_{vl}

The voltage loop clock, f_{vl} is generated using a very simple hardware arragmentment shown in the voltage loop clock generator block in Fig. 5.5. As v_{comp} is the raw output of a comparator triggered on the output voltage, which contains not only ac ripple at $2f_{line}$ but also switching ripple at f_s, debouncing of this signal is critical particularly in order to retrieve a power command update clock for the digital outer voltage loop (f_{vl}) synchronous to $2f_{line}$. Debouncing can be

accomplished using common analog hysteretic comparator circuits, such as a Schmitt trigger, or using digital debouncing techniques as is used in this SCA/D implementation. Specifically, a m-bit shift register based approach similar to the debouncing described in [58] is used to generate the debounced version of v_{comp} which is identical to f_{vl}. The delay introduced by the debouncing of v_{comp} is on the order of 3-10 times $1/f_{sys}$ depending on the total noise present on the scaled V_o signal. This delay can be thought of as the propagation delay common to traditional A/Ds. As such, the SCA/D outputs values every $1/2f_{line}$ but with a propagation delay of roughly $1/mf_{sys}$. The relative size of the PFC output capacitance C to the operating power of the PFC stage (μF/W) largely determines the amount of output voltage ripple present as described by (5.1). A lower C results in higher slope transitions of the output voltage ripple across the analog comparator threshold generally resulting in less noise on the v_{comp} signal. The length of the debouncing shift register (m) is set for a worst case μF/W expected which occurs at the lowest expected operating power of the PFC stage.

Generating f_{vl} from v_{comp} results in a voltage loop update clock that is synchronous to $2f_{line}$ and power command updates that occur near the zero-crossings of the input voltage and current so that minimal input current distortion is realized. When the SCA/D is saturated, f_{vl} is generated based on a minimum clock frequency of about $1/t_{overflow}$ through an arrangement of simple digital logic and signals, $t_{on,of}$ and $t_{off,of}$, from the error voltage calculator. This minimum clocking frequency requirement allows the voltage loop to resume normal operation following an SCA/D saturation condition. For instance, during the PFC startup the output voltage will be much lower than the minimum voltage that is able to be sensed using the SCA/D. The analog comparator output will be a zero during this period of operation. The t_{off} register will increment until the a value of $t_{overflow}$ is reached which will trigger a clocking of the voltage loop and will reset the t_{on} and t_{off} registers. For universal input PFC design, the minimum voltage loop frequency should be set marginally lower than the expected $2f_{line}$.

5.1.5 Implementation of the SCA/D

Careful consideration was given to the specific implementation of the prototype SCA/D in order to minimize measurement errors while still achieving a simple solution requiring minimal digital hardware and a low frequency system clock (f_{sys}). The precision and the propagation delay, as described in the above section, are both dictated by f_{sys}. The precision of SCA/D is a function of how accurately the duty cycle of v_{comp} can be measured. As shown in (5.8), $V_e[n]$ is calculated using both the measured t_{on} and t_{off} times whose precision is a function of f_{sys}. The SCA/D propagation delay is due to the need to debounce v_{comp} to generate f_{sys}. This debouncing takes multiple cycles of f_{sys} to implement. However, the basic precision and propagation delay requirements of an output voltage sensing A/D for a PFC are not overly difficult to meet. The precision of the SCA/D is also influenced by the length of the two n-bit registers. These registers and f_{sys} should be coordinated so that both the t_{on} and t_{off} register values are approximately $2^{(n-1)}/2^n$ when the PFC is operating in regulation and the line frequency is at a minimum. Furthermore, $t_{overflow}$ should be set so than the minimum voltage loop clocking rate is just slightly lower than the expected minimum line frequency.

The SCA/D prototype requires a total of 617 equivalent logic gates as reported from Xilinx ISE 8.2i to implement the error voltage calculator and the voltage loop clock generator. The digital hardware was implemented on a Xilinx Virtex IV FPGA. The t_{on} and t_{off} registers are 8-bits in length. With $V_K = 16V$ (from (5.4)) the SCA/D has a LSB resolution of about 2V at full power. A 5-bit shift register was implemented in the voltage loop clock generator debouncing circuit. A system clock frequency (f_{sys}) of 24.4kHz was used. The minimum voltage loop clocking frequency was approximately 95.7Hz.

5.1.6 Implemented SCA/D's Describing Function and the Effects of Saturation

A describing function is often used to describe the effective gain characteristics of nonlinear elements such as A/Ds [59]. The sinusoidal describing function of the SCA/D for various power

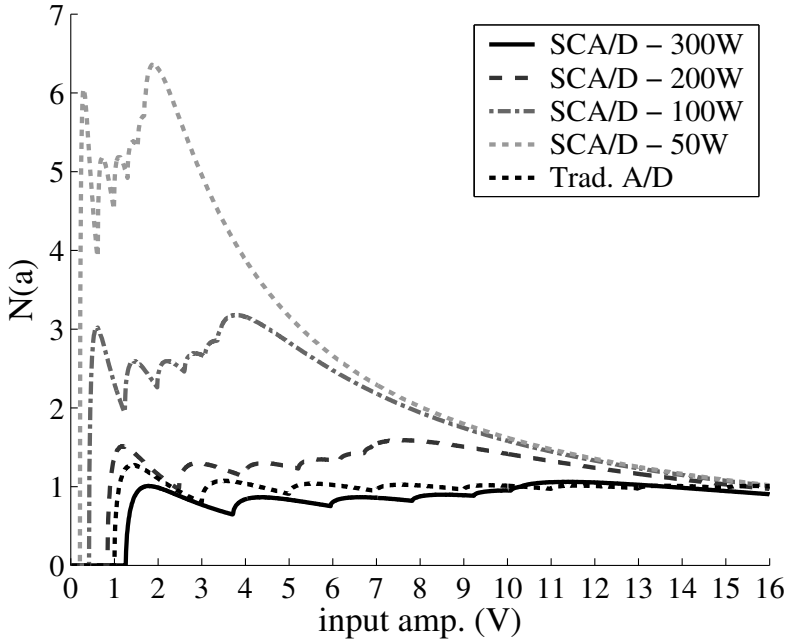


Figure 5.6: Describing function of the SCA/D and traditional A/D at $f_{line} = 60$Hz.

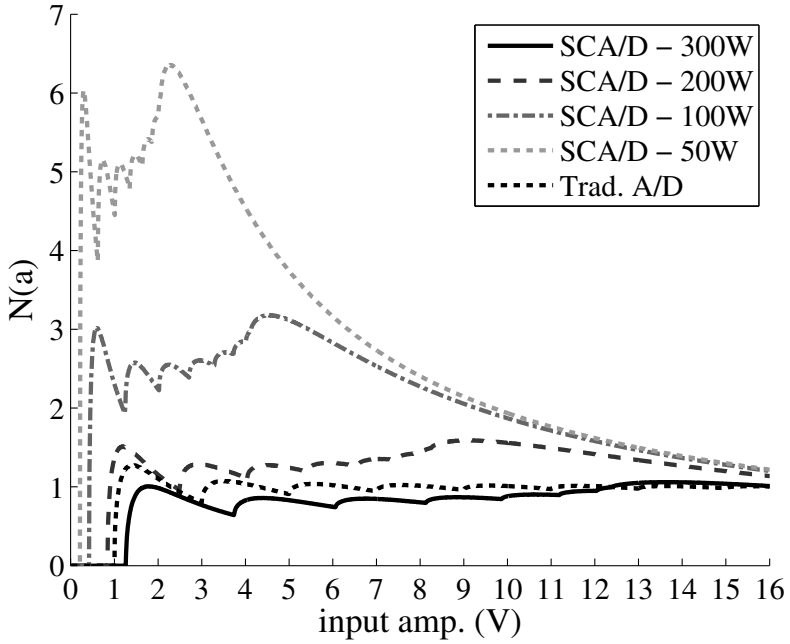


Figure 5.7: Describing function of the SCA/D and traditional A/D at $f_{line} = 50$Hz.

levels has been determined numerically in MATLAB by calculating the ratios of the fundamental components of the quantized A/D output and a sinusoidal input perturbation with swept amplitude. Fig. 5.6 shows the results of such a calculation for the SCA/D described in the above sections with $V_K = 16$V and a 2V ideal quantization level at full rated power. The describing function is shown for operating power levels of 300, 200, 100 and 50W and a line frequency of 60Hz. The describing function is also shown for a traditional A/D with 2V quantization for comparison. Fig. 5.7 shows the calculated describing functions at a line frequency of 50Hz showing the subtle effects of the SCA/D gain dependency on line frequency as described by (5.8).

As shown in Figs. 5.6 and 5.7 the describing functions for the SCA/D display the effects of saturation of the converter particularly at lower operating powers. For the PFC stage parameters given in Fig. 5.1 and a line frequency of 60Hz, the SCA/D begins to saturate at an error voltage magnitude of 10.3, 6.9, 3.4, and 1.7V for operating powers of 300, 200, 100 and 50W respectively. At a line frequency of 50Hz the SCA/D begins to saturate at an error voltage magnitude of 12.4, 8.3, 4.1 and 2.1V for the respective power levels given above. The saturation of the SCA/D for both line frequencies results in a typical $1/x$ type gain response common to all saturated A/D converters.

5.2 Power Feedforward

One of the features of the SCA/D is that a power feedforward term is inherently embedded in its operation. The small signal gain of the SCA/D is described in this section to show how the gain is dependent on the operation power of the PFC stage. Referring to (5.3) the implemented SCA/D small signal gain ($\partial V_e[n]/\partial d_{comp}[n]$) is determined by linearizing the equation by partial differentiation and evaluating the result around the regulation point ($d_{comp}[n] = 0.5$). The implemented SCA/D gain is

$$\left.\frac{\partial V_e[n]}{\partial d_{comp}[n]}\right|_{d_{comp}[n]=0.5} = 2V_K \tag{5.9}$$

Similarly the gain from d_{comp} to actual error voltage ($V_{e,actual}$) is found by linearizing and evaluating (5.2) and then taking the reciprocal. The resulting gain is

$$\left.\frac{\partial V_{e,actual}}{\partial d_{comp}}^{-1}\right|_{d_{comp}=0.5} = \frac{1}{\Delta v_o \pi} \tag{5.10}$$

Multiplying (5.9) and (5.10) together gives the complete SCA/D small signal gain from $V_{e,actual}$ to reported error voltage $V_e[n]$ as shown below.

$$\frac{\partial V_e[n]}{\partial V_{e,actual}} = \frac{2V_K}{\Delta v_o \pi} \tag{5.11}$$

Substitution of (5.1) for Δv_o yields

$$\frac{\partial V_e[n]}{\partial V_{e,actual}} = \frac{8V_K f_{line} C V_{o,rms}}{P} \tag{5.12}$$

The above relation shows that the SCA/D has a small signal gain that is inversely proportional to the operating power (P) of the PFC stage. This phenomena is also shown in the describing functions in Figs. 5.6 and 5.7. Referring to Fig. 5.6, the average gain before saturation of the SCA/D describing function for operation at 300W is about 0.8 due to the line frequency dependent scalar. At an operating power of 50W, six times lower than 300W, the SCA/D describing function shows an average gain roughly six times higher than at 300W resulting in a gain of about 4.8. This six fold increase in gain demonstrated by the inspection of the SCA/D describing function mirrors the expected operating power dependency of the SCA/D small signal gain given in (5.12).

Table 5.2: Control-to-output dc gain and dc loop gain of the voltage loop when the SCA/D is implemented.

Controller	G_{vu0}†	T_{vl0}†
ACM	$\frac{V_{o,rms}V_{g,rms}^2}{2PR_s}$	$\frac{8V_K f_{line} C V_{o,rms}^2 V_{g,rms}^2}{2P^2 R_s} \cdot G_{vc0}$
NLC	$\frac{-PV_{o,rms}^2 R_s}{3V_{g,rms}^2}$	$\frac{-8V_K f_{line} C V_{o,rms}^3 R_s}{3V_{g,rms}^2} \cdot G_{vc0}$

† results are for resistive load, no V_g feedforward

Careful consideration of the implemented current controller is necessary to realize a useful power feedforward mechanism when utilizing the SCA/D. Table 5.2 shows the dc gain of the control-to-output transfer functions (G_{vu0}) for both the ACM and NLC current control approaches when

modeled as an ideal rectifier [45]. The dc loop gain of the outer voltage loop (T_{vl0}) is also given in the table by multiplication of G_{vu0}, the voltage loop compensator dc gain (G_{vc0}) and the SCA/D gain (5.12). Inspection of Table 5.2 reveals that the dc gain of ACM PFC architectures is inversely proportional to P and that the dc gain of NLC architectures is proportional to P. Implementing the SCA/D with an ACM controlled stage results in an increase in voltage loop dc loop gain variation than if a traditional A/D were implemented. This would require a compensator design that limits the attainable bandwidth across the operating power range of the voltage loop compared to if a traditional A/D was utilized. However, an NLC controlled PFC paired with the SCA/D results in a voltage loop dc loop gain (T_{vl0}) that is fully compensated for variations in P allowing a compensator design that reduces the amount of bandwidth variation across the operating power range.

The power feedforward mechanism of the SCA/D paired with a NLC controlled current loop is analogous to the input voltage feedforward often implemented in average current mode PFC controller. The aim of both feedforward topologies is to decrease the dc gain variation in the outer voltage loop. This reduction allows for the implementation of more optimal compensators with less variation in bandwidth across the operating power range. The power feedforward mechanism of the SCA/D paired with an NLC current controller is likely to be more effective in practice at reducing overall voltage loop bandwidth variation at different operating points than an ACM controlled stage with the commonly implemented input voltage feedforward. This is due to the fact that the gain variation due to the rms input voltage residing anywhere in the universal input voltage range of 85 to 265V is about 10 whereas the power variation between full load and light load operation can be very large with a typical value being 20 when a PFC stage rated for 300W is operated at 15W for example.

5.3 Experimental Results

A single 300W boost PFC prototype was constructed with specifications as shown in Fig. 5.1. The current loop controller for the prototype was capable of operating under either ACM or NLC control. The implemented digital voltage loop could be closed using either the SCA/D or a tra-

ditional 8-bit A/D. The digital voltage loop incorporating the traditional A/D was operated synchronously at $2f_{line}$ though the use of either a zero crossing detection circuit (analog ACM control) or the line synchronization method described in Section 3.2 (digital NLC control). The digital voltage loop implemented with the SCA/D was clocked by f_{vl} as described in Section 5.1.4.

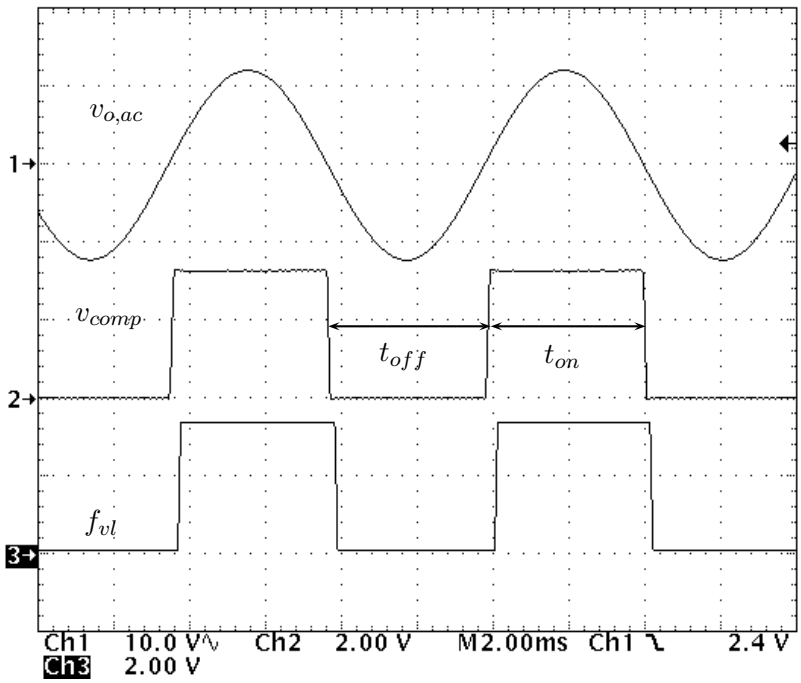


Figure 5.8: Steady-state voltage loop waveforms, $V_{g,rms} = 120$V, 60Hz, $P = 300$W.

5.3.1 Comparator Signal Conditioning

Fig. 5.8 shows the ac coupled output voltage and the accompanying comparator output (v_{comp}). In steady state the comparator output does show a duty cycle near 50% as expected from the conceptual SCA/D operation shown in Fig. 5.2(a). Also shown in Fig. 5.8 is the debounced version of v_{comp}, f_{vl}, with time periods t_{on} and t_{off} labeled. These signals are shown in detail in Fig. 5.9 along with the 24.4kHz digital system clock (f_{sys}) used to over-sample the comparator output via the t_{on} and t_{off} incrementing registers. Debouncing of the comparator output is necessary due to the presence of high-frequency noise on the scaled output voltage ($H_v V_o$) signal.

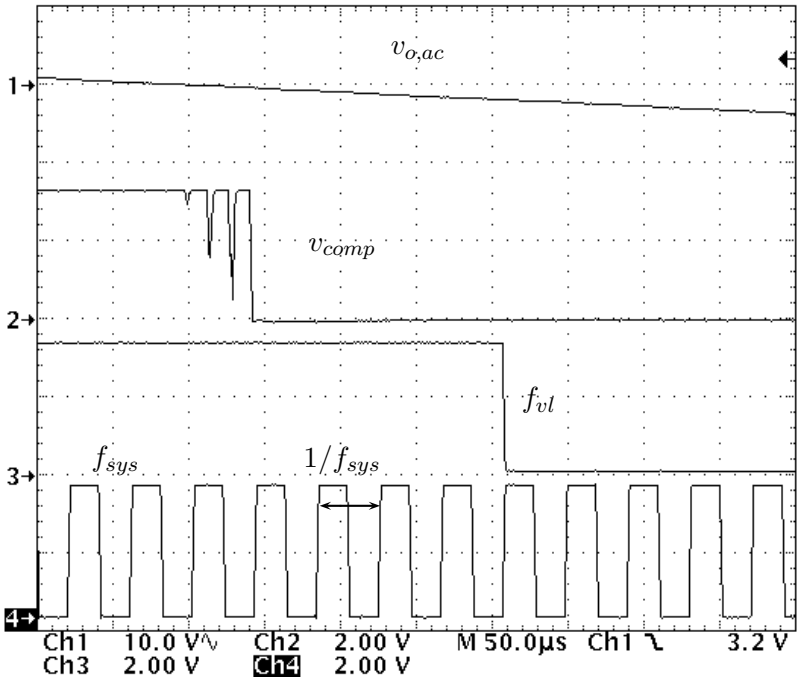
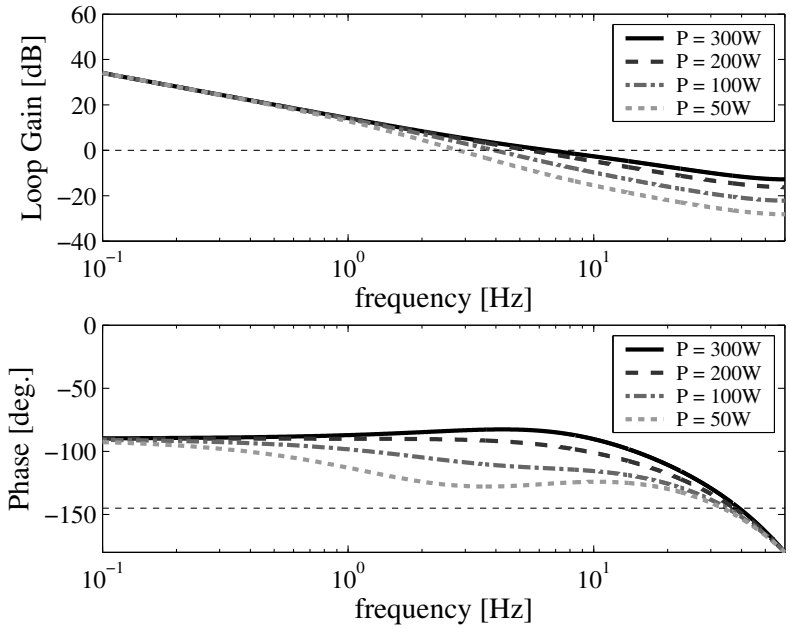


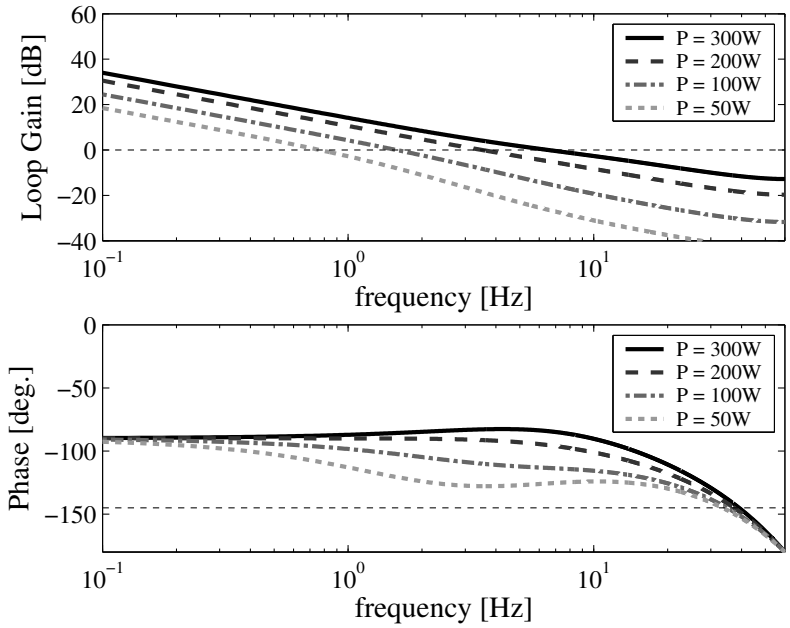
Figure 5.9: Generation of the voltage loop clock f_{vl} from v_{comp} by debouncing.

5.3.2 Outer Voltage Loop Bandwidth Improvement

The purpose behind implementing a power feedforward mechanism is to ultimately improve the line and load transient response of the outer voltage loop over a wide operating range. Fig. 5.10(a) shows the resulting loop gain and phase for the outer voltage loop with an implemented SCA/D for the PFC stage shown in Fig 5.1. The loop gain and phase is plotted for several operating power levels. Examination of this figure shows that the dc loop gain is constant for any operating power level. However, the cross over frequency and phase margin of the loop gain at different power levels are not the same. This is due to the movement of a pole in the ideal rectifier model that is dependent on the operating power of the stage. As the power of the PFC stage decreases the pole moves to lower frequency degrading both the outer voltage loop bandwidth and phase margin. For comparison Fig. 5.10(b) shows the loop gain and phase for an NLC controlled stage with a traditional A/D. Notice that the dc loop gains are now different as would be expected without a power feedforward compensation implemented. Also notice that the overall bandwidth at lower



(a) Digital voltage loop implemented using the SCA/D.



(b) Digital voltage loop implemented using a traditional A/D.

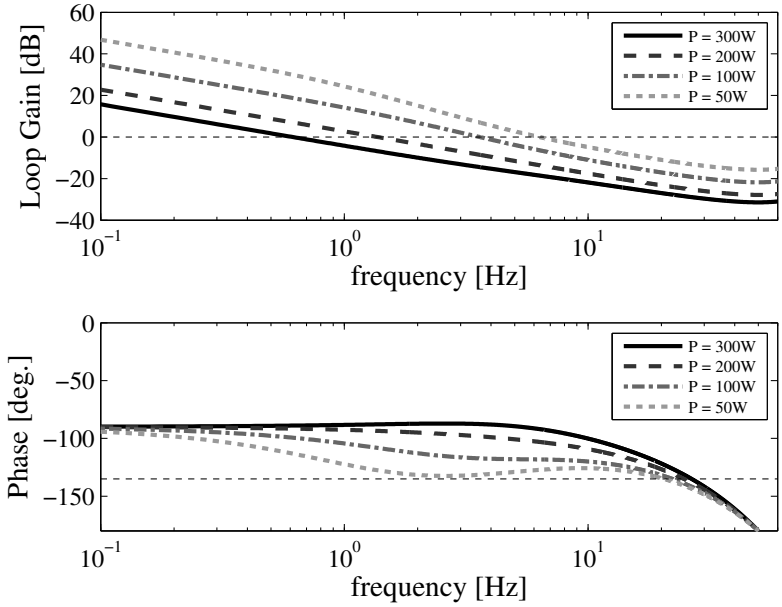
Figure 5.10: Loop gain and phase of the outer voltage loop of an NLC controlled PFC stage, $V_{g,rms} = 120\text{V}$, $f_{line} = 60\text{Hz}$.

operating powers is diminished compared to the NLC stage paired with the SCA/D. The voltage loop compensators implemented for the SCA/D and the traditional A/D loop gain plots are not identical but were designed so that both loop gains have the same bandwidth and phase margin at rated power. Table 5.3 summarizes the bandwidth and phase margin differences between the two outer voltage loops implemented with either the SCA/D or a traditional A/D. The bandwidth of the voltage loop implemented with the SCA/D is considerably improved at lower operating powers with the greatest demonstrated improvement being 3.7 times the bandwidth achieved with a traditional A/D at an operating power of 50W.

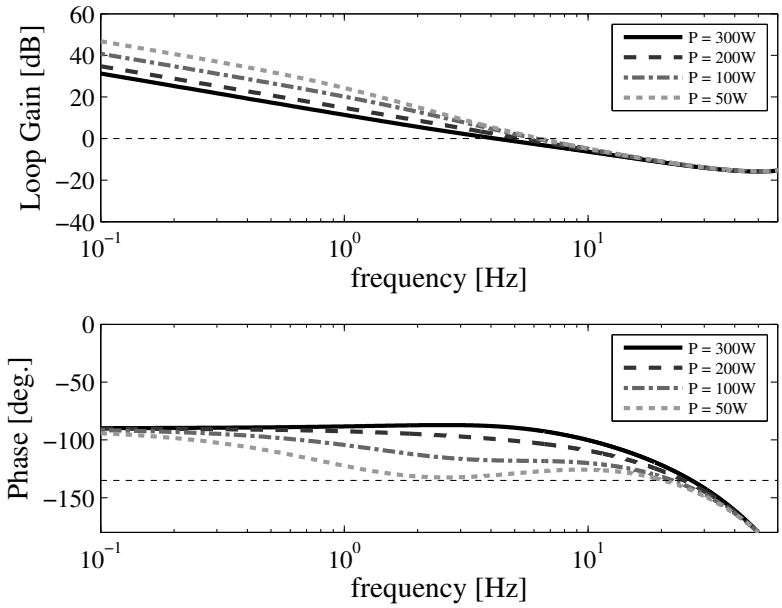
Table 5.3: Comparison of closed-loop bandwidth and phase margin of digital outer voltage loops implemented using either a SCA/D or a traditional A/D and NLC current control.

	SCA/D		Trad. A/D		
P_{load}	BW_{CL}	Φ_M	BW_{CL}	Φ_M	BW_{ratio}
300W	6.53Hz	96°	6.52Hz	96°	1.0
200W	5.44Hz	86°	3.51Hz	89°	1.6
100W	3.94Hz	69°	1.57Hz	78°	2.5
50W	2.82Hz	53°	0.77Hz	71°	3.7

For completeness the bandwidth variation increase was investigated for the case of the SCA/D being used with an average current mode (ACM) controlled PFC rectifier. For this case two voltage loops, one for use with the SCA/D and one for use with a traditional A/D, were designed so that both closed voltage loops had the same bandwidth and phase margin at an operating point of $V_{g,rms} = 230$V and $P = 50$W. Figs. 5.11(a) and 5.11(b) show the loop gain and phase for an ACM controlled rectifier paired with a SCA/D or a traditional A/D respectively. The dc loop gain is not constant in either plot and the dc loop gain variation is increased when the SCA/D is implemented as expected from the dc loop gain equation given in Table 5.2. The cross-over frequencies for the ACM paired with a traditional A/D are closely grouped due to the movement of the ideal rectifier pole to lower frequencies as the operating power decreases. The gain of the ACM stage also increases with decreasing power effectively reducing the realized bandwidth variation.



(a) Digital voltage loop implemented using the SCA/D.



(b) Digital voltage loop implemented using a traditional A/D.

Figure 5.11: Loop gain and phase of the outer voltage loop of an ACM controlled PFC stage, $V_{g,rms} = 230\text{V}$, $f_{line} = 50\text{Hz}$.

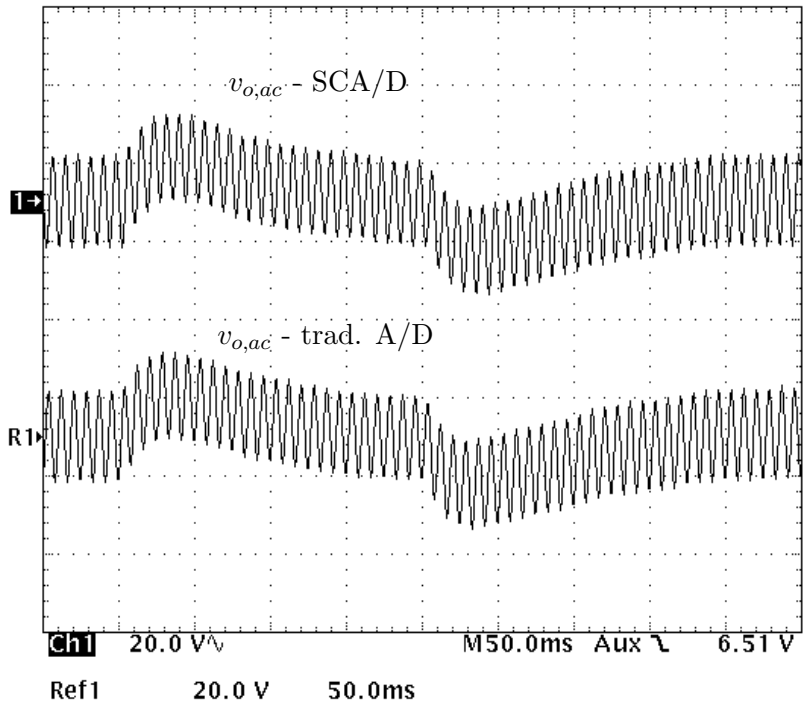
The gain variation due to operating power is increased by the power variable gain of the SCA/D resulting in lower realized bandwidths at higher operating powers. Table 5.4 summarizes the closed loop bandwidths and phase margins for the ACM controlled PFC rectifier when the output voltage is sensed with either a SCA/D or a traditional A/D. The BW_{ratio} in this table is the ratio of the traditional A/D bandwidth to the SCA/D bandwidth. In this example design the bandwidth variation across the demonstrated power range is increased nearly three fold by the SCA/Ds power feedforward mechanism. This emphasizes the importance of pairing the SCA/D with an NLC controlled current stage in order to achieve a beneficial decrease in bandwidth variation over the operating power range as opposed to a detrimental bandwidth variation increase.

Table 5.4: Comparison of closed-loop bandwidth and phase margin of digital outer voltage loops implemented using either a SCA/D or a traditional A/D and ACM current control.

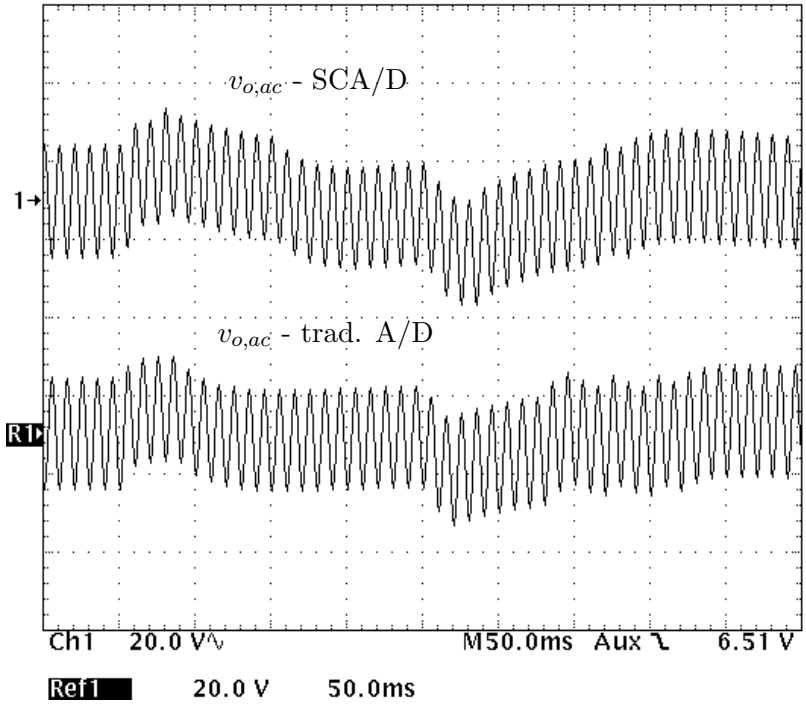
	SCA/D		Trad. A/D		
P_{load}	BW_{CL}	Φ_M	BW_{CL}	Φ_M	BW_{ratio}
300W	0.61Hz	91°	4.17Hz	92°	6.8
200W	1.37Hz	87°	5.32Hz	79°	3.9
100W	3.59Hz	63°	6.11Hz	62°	1.7
50W	6.32Hz	53°	6.32Hz	53°	1.0

5.3.3 Load Transient Responses

Waveforms showing the ac coupled output voltage response to a 30W load transient at an initial operating power of 300W is presented in Figs. 5.12(a) and 5.12(b) for input voltages of 120V, 60Hz and 230V, 50Hz respectively. The current loop is under analog ACM control and an identical integral compensator was implemented for both of the voltage loops compared. The output voltage error is digitized with either a SCA/D or a traditional A/D. At an operating power of 300W the SCA/D gain is set according to (5.4) so the value of the reported error voltage ($V_e[n]$) is nearly equal to the actual error voltage (V_e). This results in transient responses that are remarkably similar when comparing the different A/D implementations at either operating input voltage and



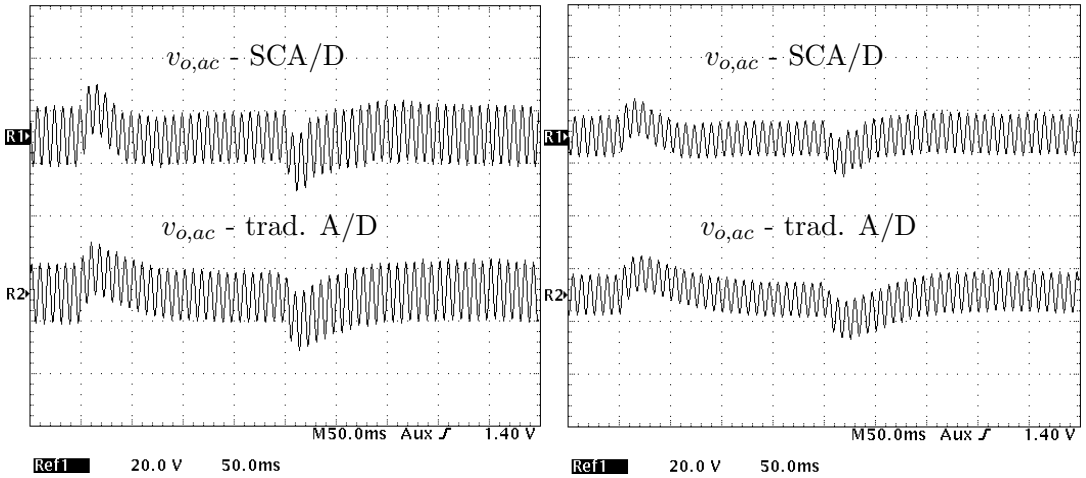
(a) Load transient responses at $V_{g,rms}$ = 120V, 60Hz, P = 300W → 270W → 300W.



(b) Load transient responses at $V_{g,rms}$ = 230V, 50Hz, P = 300W → 270W → 300W.

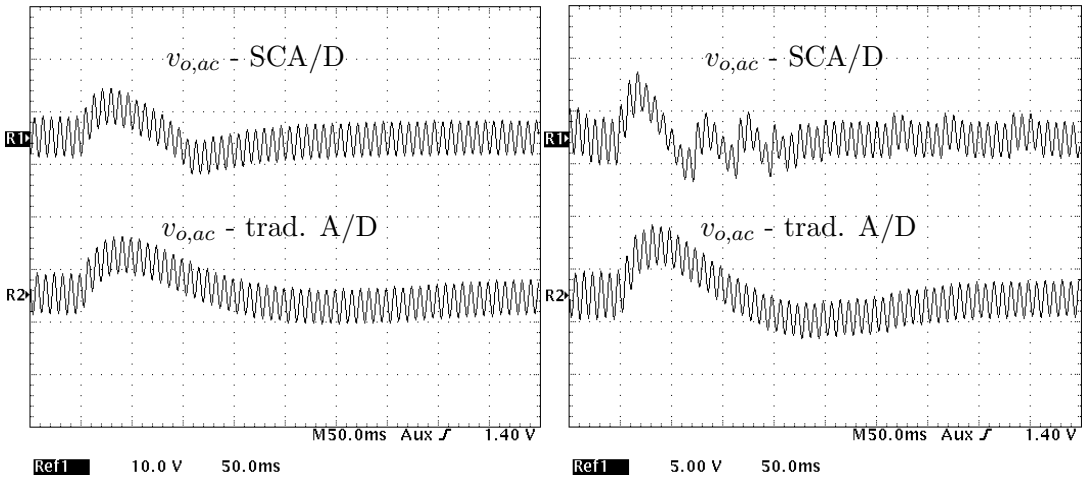
Figure 5.12: Load transient comparisons between the SCA/D and a traditional A/D with a ACM controlled PFC rectifier.

line frequency pair. These waveforms demonstrate that the SCA/D does work with a ACM type controller current loop although voltage bandwidth variation is increased as discussed in Sec. 5.3.2. Furthermore, the transient response waveforms shown in Fig. 5.12 confirm the basic operation of the implemented SCA/D when the approximate dc gain of the SCA/D is unity.



(a) Output voltage loop responses to load transients of $P = 300\text{W} \rightarrow 250\text{W} \rightarrow 300\text{W}$.

(b) Output voltage loop responses to load transients of $P = 200\text{W} \rightarrow 170\text{W} \rightarrow 200\text{W}$.

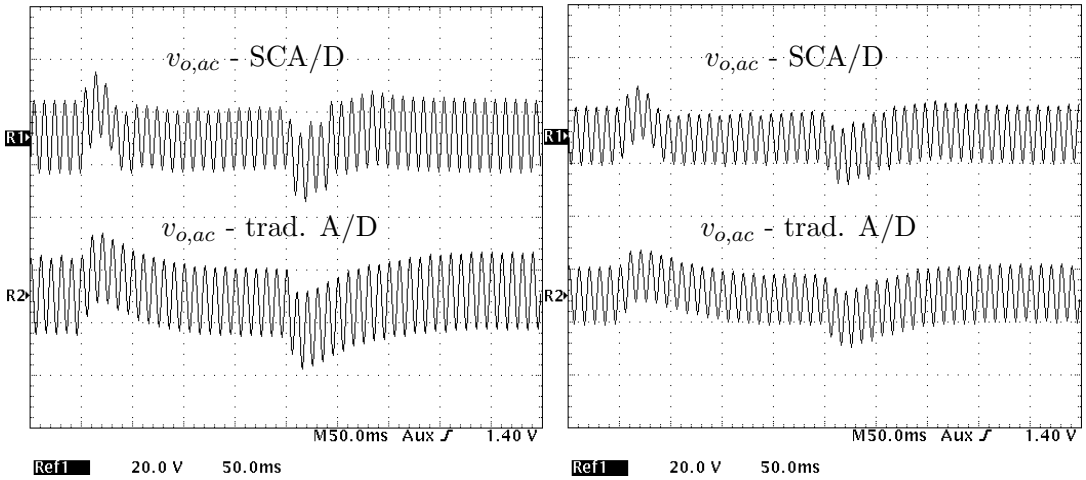


(c) Output voltage loop responses to load transients of $P = 100\text{W} \rightarrow 85\text{W}$.

(d) Output voltage loop responses to load transients of $P = 50\text{W} \rightarrow 40\text{W}$.

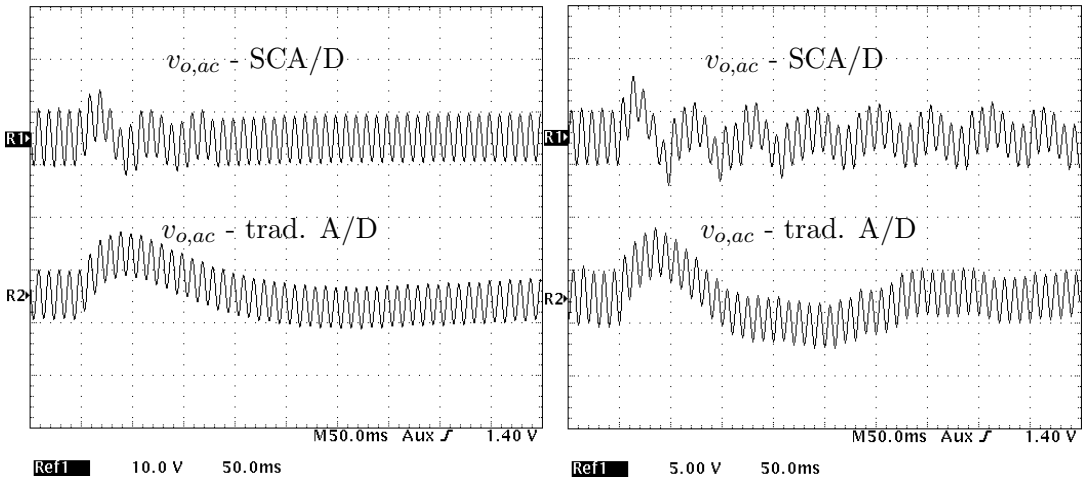
Figure 5.13: Output voltage loop response to a load transient using either the SCA/D or a traditional A/D for the NLC PFC, $V_{g,rms} = 120\text{V}$, 60Hz.

Two sets of output voltage waveforms resulting from load transients for an NLC controlled PFC paired with the SCA/D is shown in Figs. 5.13 and 5.14 for input voltages of 120V, 60Hz and



(a) Output voltage loop responses to load transients of $P = 300\text{W} \rightarrow 250\text{W} \rightarrow 300\text{W}$.

(b) Output voltage loop responses to load transients of $P = 200\text{W} \rightarrow 170\text{W} \rightarrow 200\text{W}$.



(c) Output voltage loop responses to load transients of $P = 100\text{W} \rightarrow 85\text{W}$.

(d) Output voltage loop responses to load transients of $P = 50\text{W} \rightarrow 40\text{W}$.

Figure 5.14: Output voltage loop response to a load transient using either the SCA/D or a traditional A/D for the NLC PFC, $V_{g,rms} = 230\text{V}$, 50Hz.

230V, 50Hz respectively. The output voltage waveforms resulting from various load transients are shown for a voltage loop closed using either the SCA/D or the traditional A/D. In this case, the voltage loop compensators in both implemented voltage loops are not identical but the resulting loop gains have the same bandwidth and phase margin characteristics as shown in Table 5.3. At full rated power ($P = 300$W) the two implemented voltage loops have nearly the same bandwidth and phase margin. Examination of either Fig. 5.13(a) or Fig. 5.14(a) shows that the voltage loop responses of both voltage loops are similar at rated power. Like the transient responses shown in Fig. 5.12 the gain of the SCA/D and the traditional A/D are very nearly the same at these operating points. However, as the operating power decreases, as shown in Figs. 5.13(b), 5.13(c) and 5.13(d) for a line voltage of 120V, 60Hz and Figs. 5.14(b), 5.14(c) and 5.14(d) for a line voltage of 230V, 50Hz, the voltage loop closed with a SCA/D begins to show an improved response. This improved response is due to the power feedforward mechanism of the SCA/D discussed in Sec. 5.2. Inspection of Figs. 5.13(d) and 5.14(d) reveals limit cycling of the outer voltage loop for the voltage loop closed by the SCA/D operating at low power levels. This is due to the effective reduction of the zero-error bin voltage range, $q_{A/D}$ in (4.4), of the SCA/D as operating power decreases. At 300W the zero-error bin is about 2.5V wide whereas at 50W the zero-error bin width has decreased to about 420mV violating the no limit cycling conditions described in Chapter 4.

Increasing the resolution of the power command signal using a $\Sigma\Delta$ modulator, as in Sec. 3.2, is a possible solution to avoiding limit cycling when using a SCA/D without significantly increasing the required digital hardware to implement the digital voltage loop. When considering the no limit cycling conditions for an NLC controlled PFC with an SCA/D used for output voltage sensing the worst case limit cycling operating point is at the lowest designed rms line voltage and the lowest designed operating power that limit cycling is to be avoided. In comparison the worst case limit cycling operating point when using a traditional A/D is at the lowest designed rms line voltage and the highest operating power. The change in worst case points comes from G_{vu0} being independent of power due to the power feedforward SCA/D mechanism and the decreasing zero error bin width ($q_{A/D}$) of the SCA/D as the operating power level decreases. Limit cycling aside, the action of the

SCA/D voltage loop does return the output voltage to near the dc regulation point more quickly than the traditional A/D at these low operating power levels as expected.

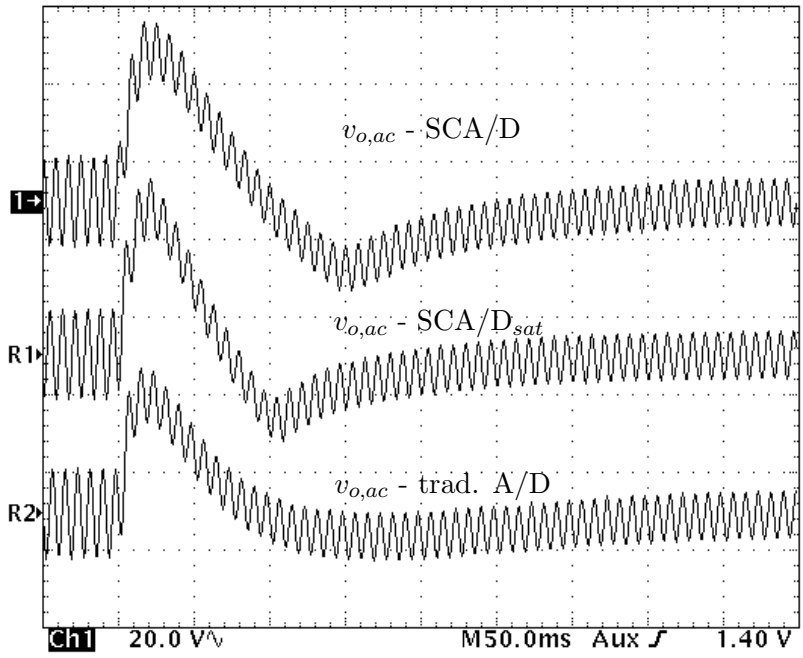


Figure 5.15: Output voltage waveforms for a large load transient, P = 300W→ 150W, $V_{g,rms}$ = 120V, 60Hz for the NLC PFC rectifier.

The ac coupled output voltage waveforms resulting from a large load transient are shown in Fig 5.15. The effects of A/D saturation are apparent in the SCA/D waveform. The load transient is large enough that the error voltage is considerably larger than the maximum reported error voltage ($V_e[n]$) of 12V for f_{line} = 60Hz resulting in SCA/D saturation. This saturation slows the voltage loop response considerably and while the voltage loop remains stable the peak output voltage and settling time both increase compared to the traditional A/D response also shown in Fig. 5.15. The traditional A/D transient response waveform shows the voltage loops response without the effects of A/D saturation or power feedforward compensation. The transient waveform labeled SCAD$_{sat}$ shows the response of a SCA/D based voltage loop with an additional nonlinear feature designed to improve transient response. In this implementation, the maximum magnitude of $V_e[n]$ is increased by 10V when the SCA/D has been saturated (i.e. reporting maximum or minimum error voltage)

for more than one half line period. As shown in Fig. 5.15, the settling time is improved to nearly match the performance of the traditional A/D. However, the peak output voltage value is not improved due largely to the one cycle delay required to detect saturation of the SCA/D. This delay results in the same peak output voltage value as with the standard SCA/D implementation.

In practice this type of non-linear control is difficult to realize in systems requiring robust operation. This is because there is an inherent lack of feedback information regarding the output voltage once the SCA/D has saturated. Adding temporal information, as demonstrated above, is the only additional information attainable regarding the state of the output voltage with the data available. However, the amount that the error voltage is above or below the SCA/D saturation rails is completely unknown. A constant correction to the error voltage amplitude will result in power dependent responses. At full operating power the constant correction will have a gain close to unity however the same constant correction will have an effective gain of six at an operating power of 50W. This power dependence limits the effectiveness of a simple constant error voltage correction during saturation.

5.4 Chapter Summary

This chapter describes a digital output voltage sensing method for use with PFC rectifiers called the single comparator A/D (SCA/D). Using a single analog comparator and simple digital hardware it is possible to estimate the output error voltage within the range of the ac output voltage ripple. A full description of the operation of the SCA/D is given as well as analysis of the converters gain and describing function. It is further shown that the SCA/D provides a beneficial power feedforward mechanism when used in conjunction with an NLC controlled current loop PFC stage. Steady-state waveforms showing proper operation and outer voltage loop gain plots showing improved achievable bandwidth at lower operating powers are presented. Additionally, a comprehensive set of load transient responses for multiple input voltage and operating power conditions is shown for both the proposed SCA/D and a traditional A/D for comparison.

Chapter 6

PFC Input Power Measurement Using Data Collected for Control Purposes

In the largely cost driven market of PFC controllers it is often difficult for IC manufacturers to market new products effectively. Existing PFC controller solutions are generally adequate to pass the required current harmonic standards and a strong case needs to be made to convince a power supply manufacturer that either spending more money on a new PFC controller or re-designing a product to incorporate a new PFC controller will be worthwhile. Value added features, controller functions that typically do not add greatly to the cost of the PFC controller but may offer a considerable benefit to the manufacturer or end user, are often used to encourage the purchase and use of emerging controllers. One such value added feature for a PFC controller is the measurement of the power consumed and processed by a PFC rectifier stage. This chapter reports an investigation regarding the measurement of the PFC stage input power based on sampled data available coincidentally in digital PFC controllers. This value added feature is specifically considered in the context of single-phase PFCs for use in data centers. Such an input power measurement implementation could allow for the more equitable division of energy and overhead costs as well as enable advanced power management systems to improve the data center efficiency.

Time-of-use (TOU) marketing strategies, where the cost of electrical energy depends on what time of day the energy is used, and the increasing need for smart power management have lead to the need for energy submetering in many energy intensive service industries. Specifically, data centers, which contain many racks of servers with each server consuming about $200-300W$ from a single phase ac line at peak operation, are interested in submetering at the server level to implement

cost-plus data services and intelligently manage power processing during lower power operation. Energy metering IC's [60–63] could be used along with shunt and series resistive networks installed at the input of a server's power factor correction (PFC) rectifier to provide an accurate measurement of power and energy usage. However, with the advent of digitally controlled PFC rectifiers it is possible to process signals already available from the digital PFC controller to provide a power measurement of reasonable accuracy with a lower implemented cost.

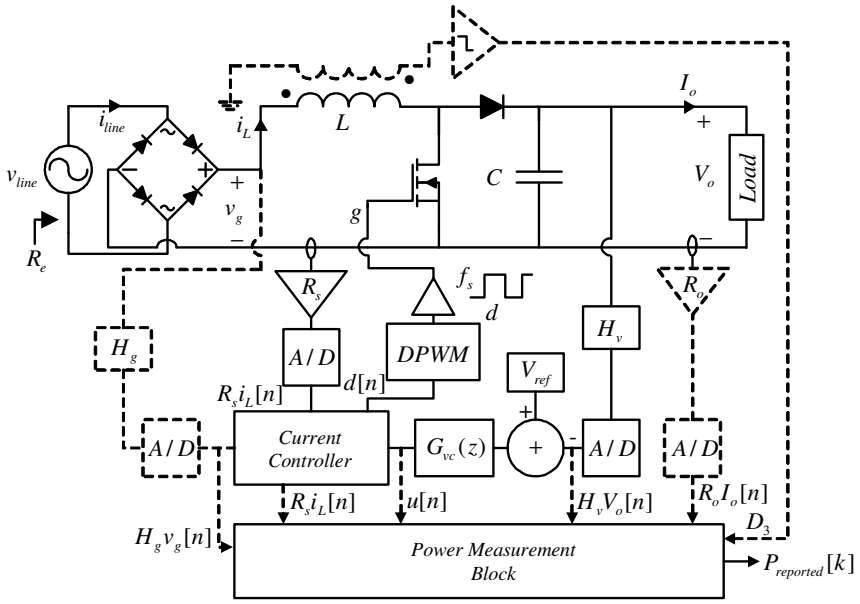


Figure 6.1: Digitally controlled PFC boost rectifier with a power measurement system.

Fig. 6.1 shows a digitally controlled PFC rectifier with the addition of a power measurement block which uses only digital information already available from the digital PFC controller or from a downstream DC-DC controller. Power factor correction is attained using either digital average current mode (DACM) [15–17] or digital nonlinear carrier (DNLC) PFC control presented in Chapter 3. The methods for generating power measurements using either control topology are described. Also, a power measurement technique is described that utilizes an output current (I_o) measurement as well as output voltage (V_o) information available in either control topology mentioned above. This technique does not require extra hardware if the PFC output current measurement is freely

available from a downstream DC-DC converter. This current would be measured for control purposes of the downstream DC-DC stage and would either be transmitted serially or in parallel to the digital PFC controller with an implemented input power measurement system. A combined controller, a single IC consisting of both a PFC controller and a downstream DC-DC converter controller, would internalize the data channel required to pass information from one controller to another reducing the difficultly of this power measurements implementation. Table 6.1 provides an overview of the three considered techniques in terms of the signals used to calculate the input power, the measured PFC stage values required for calibration and if a correction for the PFC stage efficiency is necessary.

Table 6.1: Overview of input power measurement techniques.

Input Power Meas. Technique	Signals Utilized	Values Measured for Calibration	η Correction Required
DACM PFC Rect.	i_L,v_g	P_{in}	no
DNLC PFC Rect.	i_L,u,V_o	V_o, P_{in}	yes
I_o sensing	I_o,V_o	P_{in}	yes

Section 6.1 discusses the expected errors associated with input power measurements and calibration techniques to overcome these errors. Power measurement architectures for the various control topologies are presented in Section 6.2. Experimental results comparing and contrasting the performance of the power measurement architectures are given in Section 6.3.

6.1 Power Measurement Errors and Calibration

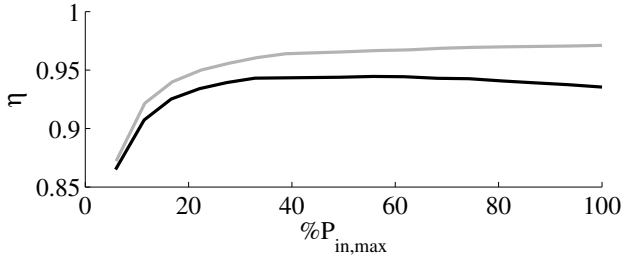
It is estimated that a relative power measurement accuracy of 2% is needed over an input power range from 20% to 100% of the maximum rated input power ($P_{in,max}$) for power submetering used for client billing. For power management purposes the accuracy may not be as important as the precision of power measurements between multiple single-phase PFC rectifiers in a system. Either implementation requires that the power measurement blocks be calibrated to adjust for hardware tolerances and imperfect input power sensing due to sensing point placement. As shown in Fig. 6.1

the signals available from the digital PFC controller are sensed after the input filter and bridge rectifier (v_g,i_L) resulting in power calculations that do not account for losses in these components. Furthermore, the basic DNLC and I_o sensing measurement techniques result in the calculation of the output power which then must be divided by the converter efficiency (η) to obtain the input power measurement desired. Since the power measurement blocks are implemented digitally there is also a small power measurement error attributable to the quantization of sensed signals.

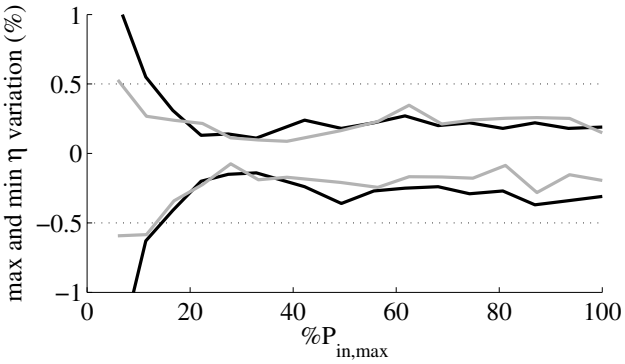
Currently, installed power measurement IC's experience a lengthy and costly calibration procedure where many data points are collected to effect an accurate calibration. The reduction of the required data collection points, thus reducing calibration time, is of utmost interest in industry in order to reduce the implemented cost of an accurate input power measurement system. It should be noted that it is possible to eliminate the need for sensor calibration by using precision sensing networks and accompanying analog to digital converters (A/Ds). However, compensation for sensing point placement would still need to be accomplished using loss models (e.g. efficiency η) to determine the input power. The focus of this research was on input power measurement techniques that will adequately determine the input power using standard tolerance sensing networks. In order to increase the accuracy of the input power measurement all proposed measurement techniques are calibrated directly against the actual input power measured using an accurate power meter. Optionally, the signals used to calculate the input power could be calibrated for their specific average or RMS value measured externally during calibration. Either method should yield similar results.

6.1.1 Indirect Input Power Measurement Using a Look-up Table

Power measurements calculated using controller data from the DNLC controller and the I_o sensing measurement technique result in the calculation of the output power (as further discussed in Section 6.2). Calibration for these techniques requires the calibration of the sensed converter signals directly, which should be completed on every production unit. The input power is then attained by dividing the output power by the converter efficiency. The converter efficiency is obtained from a look-up table (LUT) that is populated with an average efficiency at a specific



(a) Average PFC efficiency for $V_{line,rms} = 115$V (black) and 230V (gray), $n = 14$ units.



(b) Maximum and minimum PFC efficiency variation from average PFC efficiency for $V_{line,rms} = 115$V (black) and 230V (gray), $n = 14$ units.

Figure 6.2: Average η and max. and min. variation for 14 production units.

operating input voltage and output power of many tested production units. The exact efficiency of a particular production unit is not used to correct for sensing point placement but rather an averaged efficiency for that type of production model. Fig. 6.2(a) shows the averaged efficiencies for $V_{line,rms} = 115$V and 230V generated by testing 14 production units of a particular PFC stage design. The variation in the production units efficiency from the average efficiency is very low as shown in Fig. 6.2(b). Over the power measurement range of interest this variation is well below $\pm 0.5\%$. The small variation in efficiency implies that the efficiency correction data can be obtained once and stored in a look-up table for the entire production unit type, thus greatly decreasing the calibration time required for a single production unit.

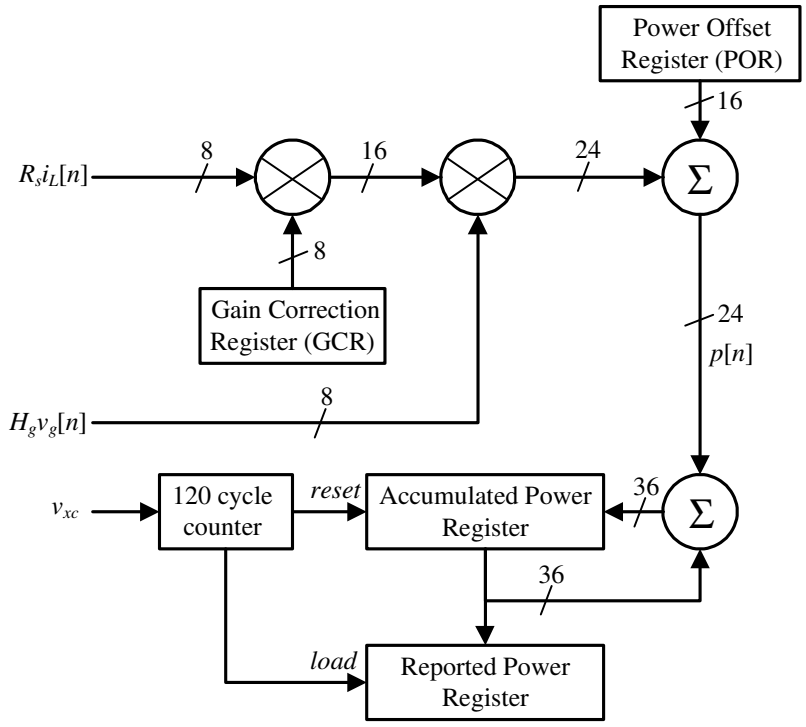


Figure 6.3: Diagram of the power measurement block for the DACM controlled PFC.

6.1.2 Gain Correction and Power Offset Registers

For both the DACM and DNLC power measurement blocks, shown in Figs. 6.3 and 6.4, two correction registers are employed to effect an accurate calibration. A signed 7-bit gain correction register (GCR) linearly scales a digital signal ($s[n]$) by the following relation.

$$s[n]_{scaled} = s[n]_{unscaled} \times \left(1 + \frac{GCR}{128}\right) \tag{6.1}$$

where the digital value for GCR can range from -64 to 63 resulting in a scaling range from 0.5 to 1.4922.

A power offset register (POR) is also utilized in the DACM power measurement block. This offset register simply adds or subtracts a constant offset from the calculated power. The corrected calculated power signal ($p[n]$) is then accumulated over 120 half line cycles in order to produce the reported power which represents the average power over the last averaging period (one second when $f_{line} = 60Hz$). The resetting of the accumulated power register and the loading of the reported

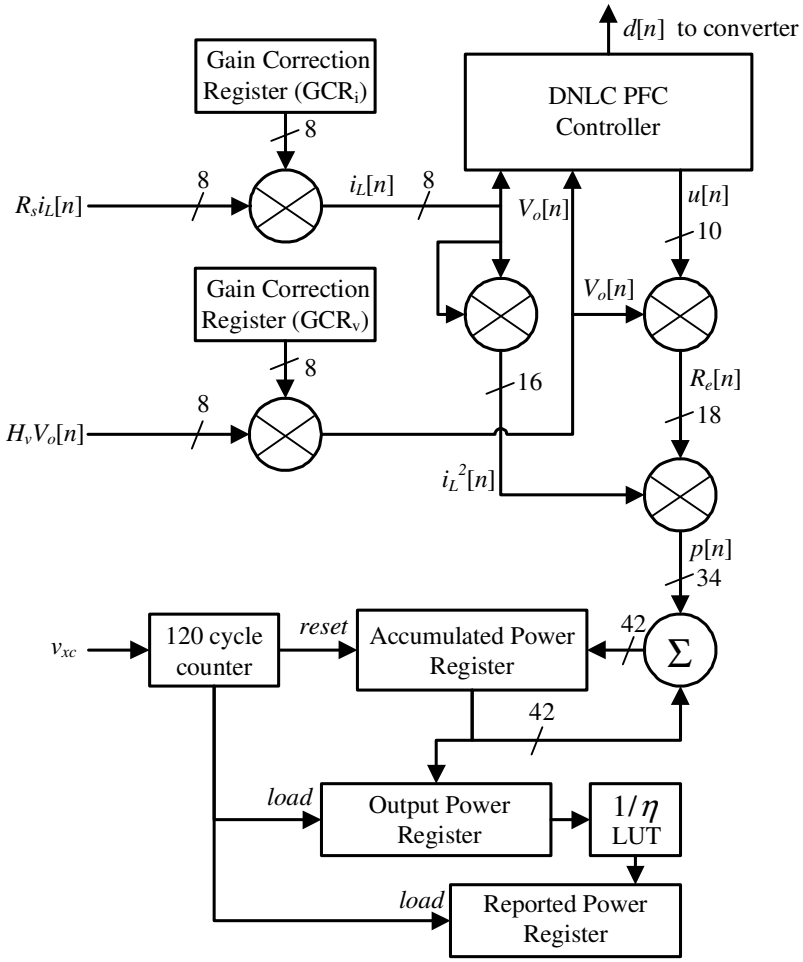


Figure 6.4: Diagram of the power measurement block for the DNLC controlled PFC.

power register are triggered by a 7-bit counter that resets at a value of 119 and is clocked with a current zero crossing synchronized clock signal (v_{xc}) from the digital PFC controller as described in Chapter 4.

6.1.3 Current Sense Correction During DCM Operation

The inductor current is sensed in the middle of the switch on-time in order to represent the average inductor current during a switching period when the converter is operating in continuous conduction mode (CCM). However, this same technique will lead to the overestimation of inductor current when the converter is operating in discontinuous conduction mode (DCM). The prototype

converter used for DACM and DNLC power measurement testing operates in DCM for part of the input current line cycle for output powers below about 60W when the line voltage is $120V_{rms}$. For a line voltage of $230V_{rms}$ the converter operates in DCM during an ever increasing percentage of the half line period as the power is reduced from full power to light load. In order to correct for the overestimation of the average inductor current during DCM operation a DCM correction (DCMC) function has been implemented, as described in [64]. The operation of this correction function requires the addition of an inductor voltage sensing comparator as shown in Fig. 6.1. The comparator output (D_3) is used to calculate the duration of the discontinuous conduction period (T_{DCM}) which is then used to scale the sensed current value so that it more closely represents the actual average current during a switching period.

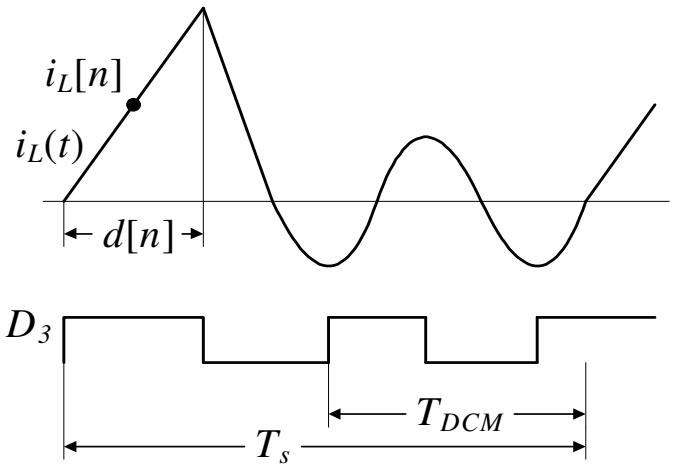


Figure 6.5: Estimation of T_{DCM} during DCM operation.

The calculation of T_{DCM} is accomplished by using a high speed clock that is enabled when D_3 transitions to a high state when the boost switch is off. This transition occurs due to the ringing present at the boost switch node when both the boost switch and the diode are not conducting. Further transitions of D_3 are ignored until the value of the high speed clock is registered when the next switching period begins. Fig. 6.5 shows the T_{DCM} calculated in this manner. Notice that the actual period that the converter is in DCM is actually longer than T_{DCM} by one quarter ringing

period. The sampled inductor current is scaled according to:

$$i_{L,DCM}[n] = \frac{T_s - T_{DCM}}{T_s} i_L[n] \tag{6.2}$$

Due to the measured T_{DCM} being shorter than the actual discontinuous conduction period the inductor current is still expected to be slightly overestimated during DCM operation. Also, this method does not account for the average inductor current component contributed by the ringing of the switch node during DCM operation.

6.2 Input Power Measurement Techniques Using Digital Control Data

Details of the three power measurement techniques summarized in Table 6.1 are discussed in this section.

6.2.1 DACM PFC Rectifier Technique

When employing DACM control the digital controller utilizes scaled versions of both the bridge voltage ($H_g v_g$) and the inductor current ($R_s i_L$) for current control purposes. Using these two values it is directly possible to calculate the instantaneous power as:

$$p_{in}[n] = \frac{v_g[n]}{H_g} \times \frac{i_L[n]}{R_s} \tag{6.3}$$

For simplicity it is assumed that H_g and R_s have effective magnitudes near unity as a result of attempting to digitally represent the real values of the control inputs in the digital controller. For example, the external resistor divider for v_g gives $H_{g,analog} = 1/250$. However, in the digital representation, $v_g[n]$, the radix point is placed such that the sensed signal $H_g v_g$ is "multiplied" by $2^8 = 256$, thus the effective H_g is near unity at 256/250. This type of design allows limited gain scaling networks, as described by (6.1), to be employed.

Referring to Fig. 6.1, it is apparent that power losses prior to the output of the bridge rectifier will result in the power measured at the bridge output to be lower than the actual input power. Fig. 6.6 shows an input filter and bridge rectifier loss model for RMS line voltages of 120V and

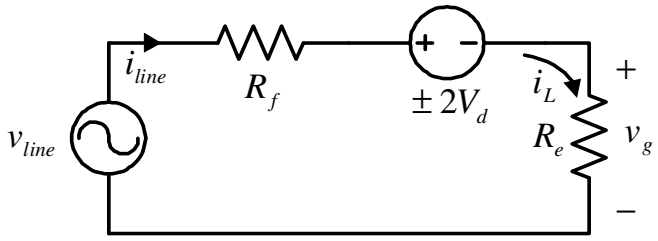


Figure 6.6: PFC input filter and diode bridge loss model.

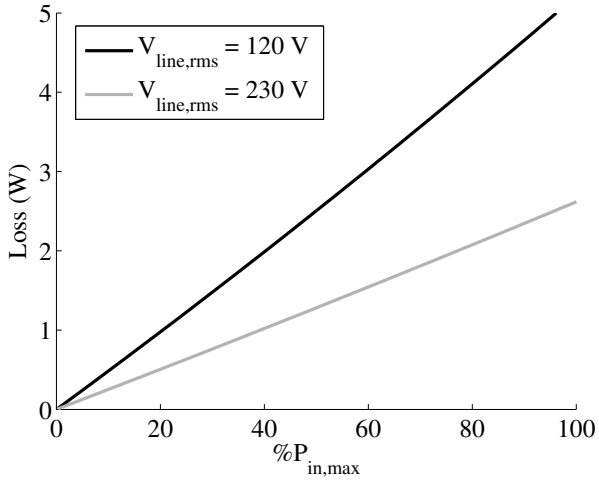


Figure 6.7: Calculated PFC input filter resistance (R_f) and diode drops ($2V_d$).

230V. The model includes losses due to the input filter resistance (R_f) and the diode voltage drops ($2V_d$). The input filter resistance is primarily due to the copper losses in the common mode choke windings typically installed in a PFC input filter. The power dissipated by the input filter and the diode bridge is defined as:

$$\langle P_{loss} \rangle_{T_{2L}} = R_f I_{L,rms}^2 + 2V_d I_{L,avg} \tag{6.4}$$

For typical values, $R_f = 58\text{m}\Omega$ and $V_d = 1\text{V}$, Fig. 6.7 indicates that the linear diode losses are dominant inferring that the input filter and diode bridge losses can be compensated using a linear gain correction of the inductor current. Since a gain correction is already required to calibrate for the sensing tolerance of the inductor current this power measurement method is a good candidate for calibrating the power measurement block output directly for the input power of the PFC stage.

This effectively accounts for sensor tolerances and losses prior to sensing points with a single calibration procedure.

Fig. 6.3 shows the power measurement block topology proposed for DACM controlled PFCs. The sensed inductor current, $R_s i_L[n]$, is first scaled according to the GCR and is then multiplied by the sensed bridge voltage, $H_g v_g[n]$. The POR is then added and the offset corrected power signal is averaged over 120 half line cycles and is reported via the reported power register.

Power measurement calibration is achieved by collecting two data pairs of the actual input power (P_a) and the reported power (P_r) from the DACM power measurement block with all correction registers set to zero. These data pairs are collected for each intended operational line voltage ($V_{line,rms}$) and values of $P_a \approx 0.2P_{in,max}$ and $0.75P_{in,max}$ have been found to result in a reasonably accurate calibration using this method. Using this data, the GCR is calculated by:

$$GCR = \frac{P_{a,0.75P_{in,max}} - P_{a,0.2P_{in,max}}}{P_{r,0.75P_{in,max}} - P_{r,0.2P_{in,max}}} \tag{6.5}$$

and the POR value is calculated by:

$$POR = P_{a,0.75P_{in,max}} - GCR \times P_{r,0.75P_{in,max}} \tag{6.6}$$

This calibration method ideally guarantees zero measurement error at both $0.2P_{in,max}$ and $0.75p_{in,max}$.

6.2.2 DNLC PFC Rectifier Technique

As presented in Chaper 3, the DNLC PFC control approach requires only an inductor current ($R_s i_L[n]$) and output voltage ($H_v V_o[n]$) sense for control of the PFC. A power command signal ($u[n]$) is generated and adjusted by the voltage control loop regulating the output voltage. The emulated input resistance (R_e) is related to the power command signal by the following equation modified from (3.2),

$$R_e = \frac{uV_oR_s}{\eta}. \tag{6.7}$$

where η is the average converter efficiency over a half line cycle. Using this relation and the fact that $R_s i_L[n]$, $u[n]$ and $H_v V_o[n]$ are already available in the PFC controller, the instantaneous power

of the PFC stage can be calculated by:

$$p_{in}[n] = \frac{i_L^2[n]u[n]H_v V_o[n]}{R_s \eta} \tag{6.8}$$

The above equation also shows that the immediate power measurement available by processing sensed and calculated data from the DNLC controller is actually the PFC stage output power ($\eta p_{in}[n]$). This is due to the fact that the emulated resistance (R_e) is set by the outer voltage loop that actually regulates the power stage output power not input power. In some power management functions the reporting of the output power may be sufficient for accurate system management. However, for power submetering the input power must be calculated according to (6.8) including the correction for converter efficiency (η) at that specific converter operating point. A two-dimensional look-up table has been used to provide the expected converter efficiency at any input voltage and any expected output power level. For a prototype DNLC PFC stage with a nominal power output of $P_{out,max} = 300$W a total of 143 efficiencies were collected in order to populate a 13×11 LUT ranging in output power levels from $60W$ to $300W$ and ranging in RMS input voltages from 90V_{rms} to 260V_{rms}. As discussed in Section 6.1, this LUT is not populated with a single converters expected efficiencies but rather the averaged efficiencies gathered from testing a set of production units.

The DNLC PFC's current control law requires that the power command signal $u[n]$ be limited to a maximum value due to current loop stability issues during low power and/or high line voltage operation as discussed in Section 3.1.1. While the DNLC controller continues to provide satisfactory input current waveshaping during these operating points the value that $u[n]$ represents when saturated does not accurately reflect the desired relation shown in (6.7). This is a major limitation to using DNLC control data for input power measurements for universal input designed PFCs. At high line voltages a reasonably sized inductor and chosen switching frequency results in the DNLC PFC controller operating with a saturated $u[n]$ at most if not all operating power levels. While high quality PFC current shaping is largely maintained the ability to estimate the power processing level of the PFC stage is lost entirely.

Calibration of the DNLC power measurement block entails the calibration of the inductor

current sense ($R_s i_L[n]$) and the output voltage sense ($H_v V_o[n]$). These gain corrections are made prior to the input of the DNLC PFC controller as shown in Fig. 6.4. This is necessary as accurate digital representations of i_L and V_o are required in order for the power command signal $u[n]$ to accurately relate to (6.7). First the voltage gain correction register (GOR_v) is adjusted so that the regulated output voltage matches the expected output voltage set by the DNLC outer voltage loop's voltage reference. This assures that the output voltage scaling factor H_v has been compensated by the setting of GCR_v. Secondly, the current gain correction (GCR_i) is adjusted so that the reported power matches the measured input power of the PFC stage. In this study this calibration was completed at an operating input power of $0.75P_{in,max} = 225$W for a DNLC controlled prototype that used 8-bit A/Ds to sense converter signals.

6.2.3 Output Current Sensing Technique

If an output current measurement ($R_o I_o[n]$) is available as shown in Fig. 6.1 the PFC stage input power can be determined as:

$$p_{in}[n] = \frac{H_v V_o[n] R_o I_o[n]}{\eta} \tag{6.9}$$

Like the DNLC based power measurement, without correction for converter efficiency (η) the calculated power will be equal to the output power. Again, a LUT approach is utilized to correct for converter efficiency. In this case the LUT directly outputs the expected input power value by interpolation given the reported output power (calculated by (6.9) without η correction) and the RMS line voltage. The LUT is populated with the average input power measured from a set of production units tested at various input voltages and output powers. Tests of this input power measurement technique were completed using a digitally controlled PFC with 12-bit A/Ds for sensing and a maximum input power ($P_{in,max}$) of 800W.

The I_o sensing technique relies on sensing the dc output voltage, the dc output current, and the efficiency characterization, which can be performed once for the entire type of production units, as discussed in Section 6.1.1. If accurate output current and voltage samples are available, which

is easier to realize on the output (DC) side of the rectifier, it should be noted that the input power measurement could be accomplished without the need for per-unit calibration. This is a significant advantage of the output current sensing technique.

Calibration on a unit by unit basis, if required, is much the same as described for the DACM power measurement technique. Input power and output power pairs are collected at two power levels for every intended operating line voltage. A gain scaling factor is applied either to the output current or output voltage measurement to correct for gain errors in the sensing networks. A power offset is also utilized to correct for any constant offset in either sensed signal. The offset corrected power signal is then used to determine the expected input power by interpolating the input power LUT.

6.3 Experimental Results

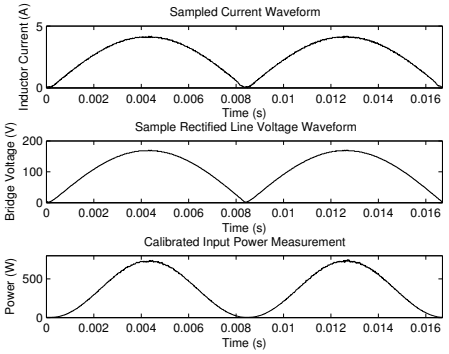
Experimental input power measurements were collected using an Agilent 6813B AC supply which reported power supplied to the PFC input to an accuracy of 0.1% with an offset of ±0.3 W. The PFC rectifier's major component values are given in Table 6.2.

Table 6.2: Input power measurement PFC stage parameters.

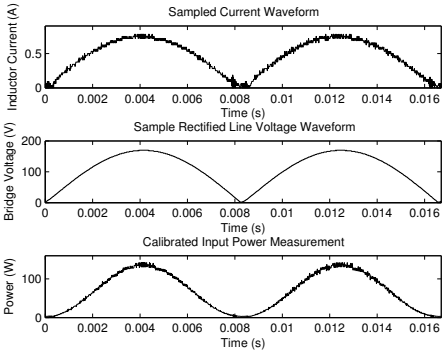
Parameter	Value
C	220μF
L	1.5mH
$V_{o,nominal}$	390V
f_s	65kHz

6.3.1 DACM PFC Rectifier Technique

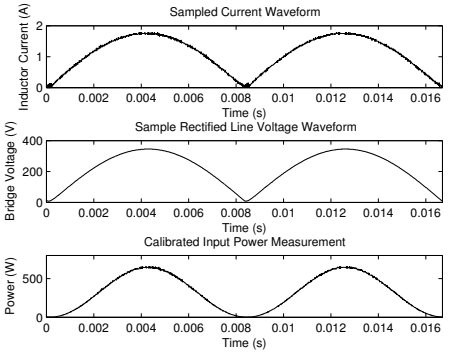
Fig. 6.8 shows sampled input and output waveforms for the DACM power measurement block for various input voltages and power settings. The scaled digital waveforms for the bridge voltage ($v_g[n]$) and inductor current ($i_L[n]$) are shown as well as the scaled digital power signal ($p[n]$) calculated by (6.3). Due to the rectified AC waveform of both $v_g[n]$ and $i_L[n]$ the power signal



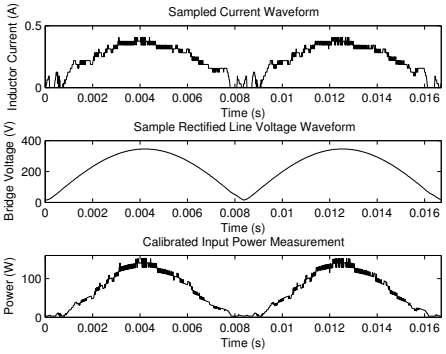
(a) Power measurement block inputs and outputs for $V_{g,rms} = 120V$ and $P_{in} = 300W$.



(b) Power measurement block inputs and outputs for $V_{g,rms} = 120V$ and $P_{in} = 60W$.



(c) Power measurement block inputs and outputs for $V_{g,rms} = 240V$ and $P_{in} = 300W$.

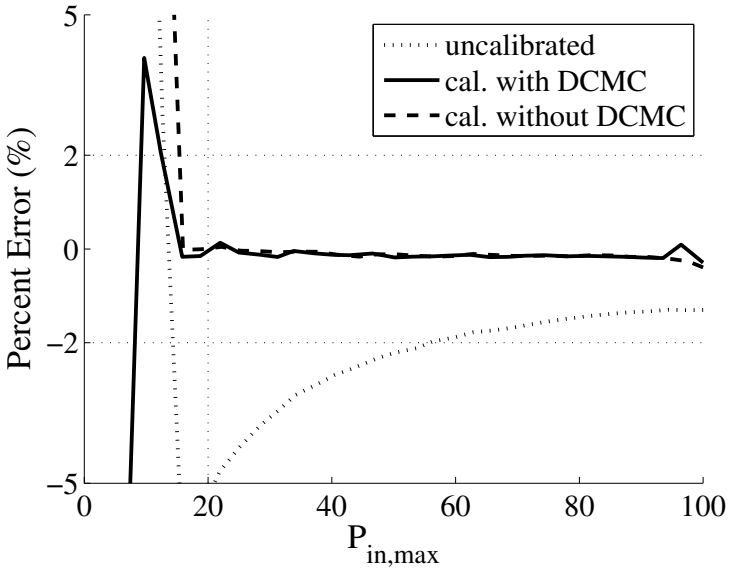


(d) Power measurement block inputs and outputs for $V_{g,rms} = 240V$ and $P_{in} = 60W$.

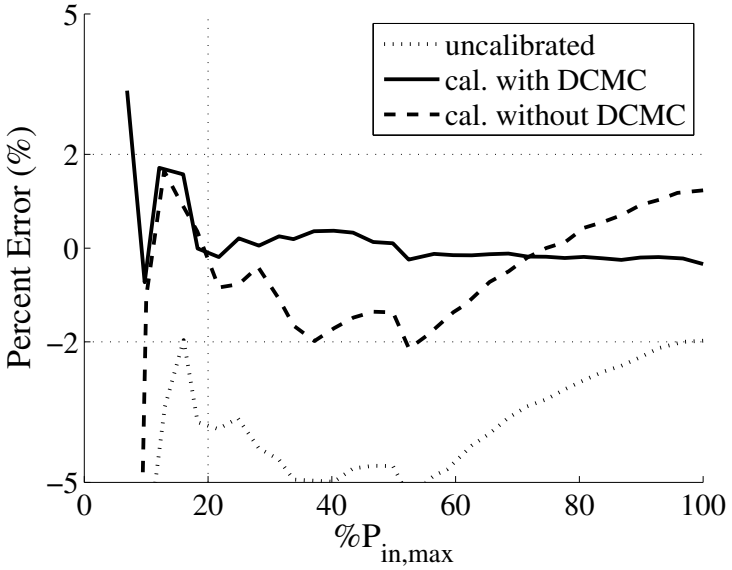
Figure 6.8: DACM power measurement block sampled inputs and outputs.

varies from zero, during zero crossings, to a maximum value equal to approximately twice the average input power. The average power is determined by integrating $p[n]$ over 120 half line cycles and dividing by the number of sample instances during the averaging time period. Integration over an integer number of half line cycles eliminates variations between reported powers during steady state operation which is essential for quick and accurate power measurements during the calibration routine.

The uncalibrated and calibrated with and without discontinuous conduction mode correction (DCMC) input power measurement relative errors are shown in Fig. 6.9 for RMS line voltages of 120V and 230V. Referring to Fig. 6.9(a) the uncalibrated error plot shows a characteristic shape where the majority of the error is caused by the need for power offset calibration. With a two



(a) Uncalibrated and calibrated with and without DCMC implemented input power measurements percent error for $V_{line,rms} = 120V$.



(b) Uncalibrated and calibrated with and without DCMC implemented input power measurements percent error for $V_{line,rms} = 230V$.

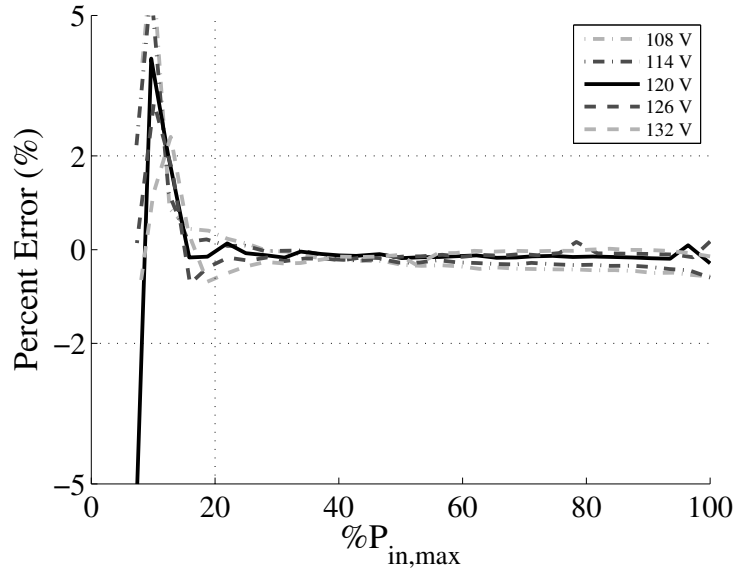
Figure 6.9: Power measurement percent error for the DACM power measurement technique.

point calibration the DACM power measurement block with or without DCMC provides adequate power measurement accuracy over the power range desired. Beyond the $0.2P_{in,max}$ boundary the converter does operate in DCM and the DCMC helps limit the power measurement percent error. Fig. 6.9(b) shows an uncalibrated error characteristic indicating the dominate need for a gain correction. Following a two point calibration the percent error is nearly bound within the desired limits. However, as the converter operates in DCM during some portion of the half line cycle over the entire power range at this voltage the addition of DCM current correction significantly increases the accuracy of the input power measurement.

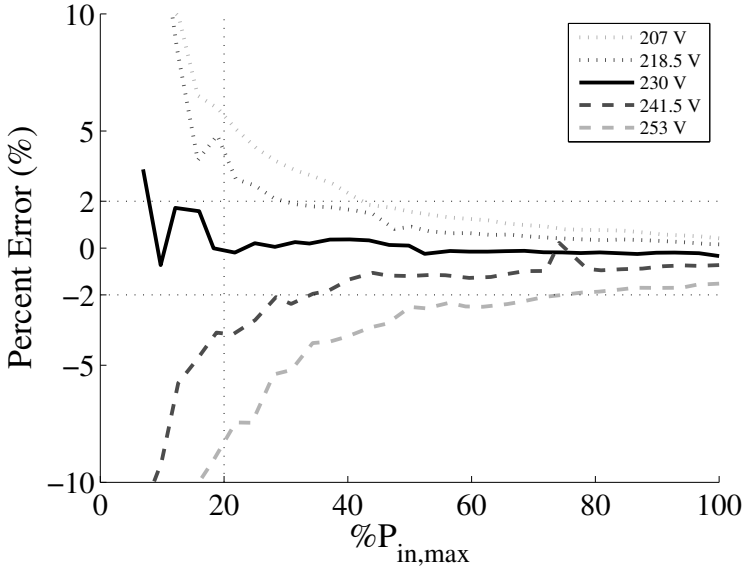
Fig. 6.10 shows the family of input power measurement percent error curves for the DACM power measurement block for line voltages of $120\text{V}_{rms} \pm 10\%$ and $230\text{V}_{rms} \pm 10\%$. In both cases the power measurement block was calibrated only at the nominal line voltage. Fig. 6.10(a) shows that the same calibration can be used over the expected line voltage variation in 120V$\pm$10% systems. The same is not true for the 230V$\pm$10% line voltage case as shown in Fig. 6.10(b). In this case higher line voltages and lower line voltages result in an underestimation and overestimation of input power respectively. This error characteristic is due to a change in quantization error introduced by the DCMC function as the converter operates in either deeper DCM or lighter DCM or more or less of the line cycle as the rms line voltage varies.

The temperature dependence of the DACM input power measurement system accuracy was also investigated. The losses realized in the input filter and the bridge rectifier were expected to be temperature dependent possibly resulting in the need to change the DACM power measurement block GCR and/or POR according to PFC stage temperature. Specifically, the aim of this testing was to determine if calibrating at a normal operating temperature of 25°C would result in a power measurement system that resulted in accurate power measurements over a large operating temperature range.

Fig. 6.11 shows a diagram of the system used to test power measurement accuracy with varying operating temperature. Testing proceeded on the DACM power measurement block by first calibrating the power measurement block at an ambient temperature of 25°C. Following calibration



(a) Input power measurement percent error for line voltage variations $120 \pm 10\%$.



(b) Input power measurement percent error for line voltage variations $230 \pm 10\%$.

Figure 6.10: Power measurement percent error for the DACM power measurement technique with line voltage variation.

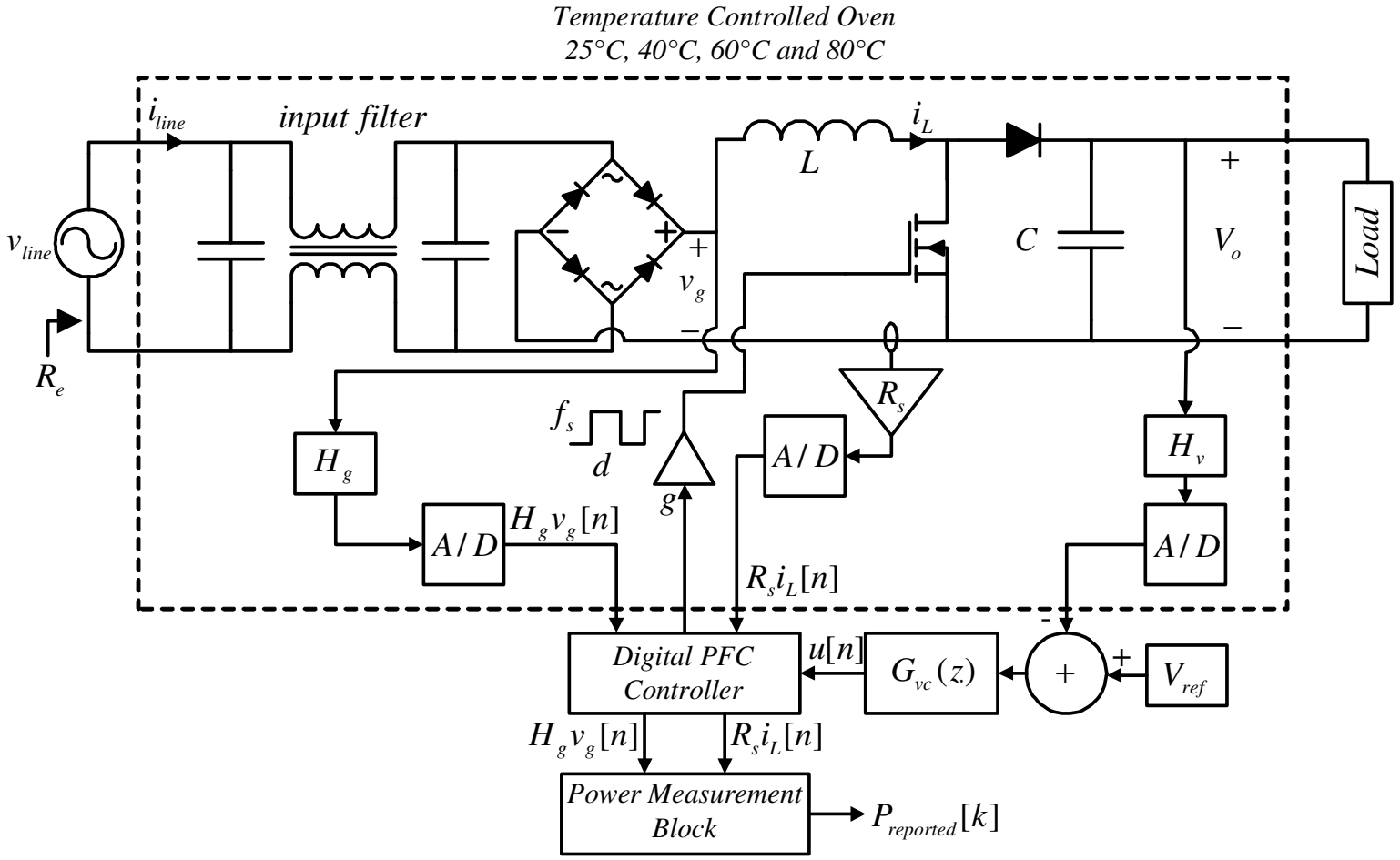
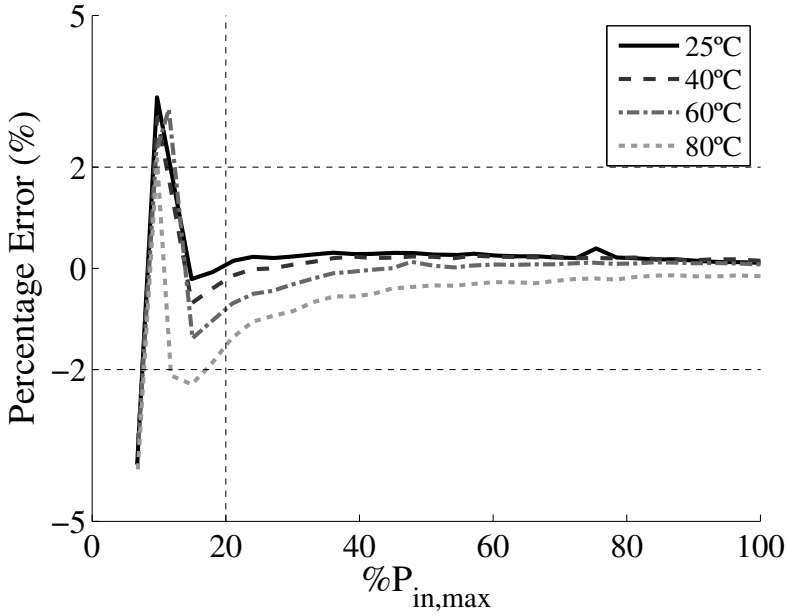
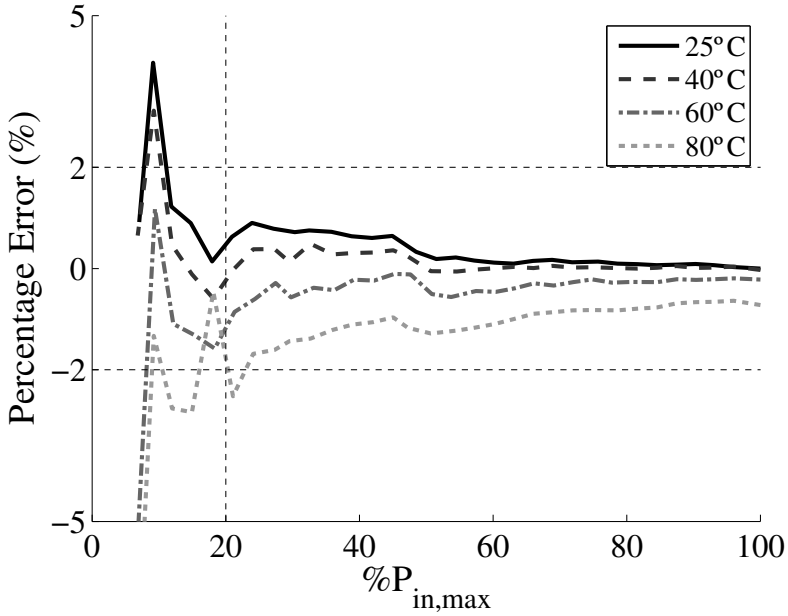


Figure 6.11: System diagram of the DACM controlled PFC under controlled power stage ambient temperature.



(a) Input power measurement percent error with changing temperature for a line voltage of 120V.



(b) Input power measurement percent error with changing temperature for a line voltage of 230V.

Figure 6.12: Power measurement percent error for the DACM power measurement technique with temperature variation.

the operating temperature of the entire power stage was controlled using a precision oven and power measurement percent error data was collected at 25°C, 40°C, 60°C and 80°C.

Fig. 6.12(a) shows the measured input power percent error for a line voltage of 120V for various operating temperatures. Over the complete tested temperature range the power measurement percent error remains within the desired 2% error range. The characteristic trend is that the reported power underestimates the actual power processed as temperature increases. The expected characteristic was that the reported power would over estimate the input power as the diode bridge efficiency was expected to improve as the diode forward voltage drops decrease with increasing temperature. The characteristic error seen in the experimental result must be due to other temperature sensitive components in the system such as gain setting resistors in the sensing networks of the rectified line voltage sense (v_g) and the inductor current sense ($R_s i_L$). Fig. 6.12(b) presents similar data for a line voltage of 230V. In this case the increased error due to the increased operating temperature at 80°C does exceed the desired tolerance band at an operating power level of about $0.25P_{in,max}$.

6.3.2 DNLC PFC Rectifier Technique

The uncalibrated and calibrated error for the DNLC power measurement technique operating at a line voltage of 120V_{rms} are shown in Fig. 6.13. Calibration is completed at a single operating power point of $0.75P_{in,max}$. The calibrated power measurement error is within the desired 2% relative error range until about $0.3P_{in,max}$ where the power command signal ($u[n]$) saturates and no longer is directly related to the emulated input resistance. This is a serious limitation as power measurement at high line voltages is not possible as $u[n]$ saturates near $P_{in,max}$ for a line voltage of 230V_{rms}.

6.3.3 I_o Sensing Technique

The I_o sensing power measurement technique was verified by testing five production units for percent error compliance after a simple two point calibration at a given line voltage. Fig. 6.14 shows

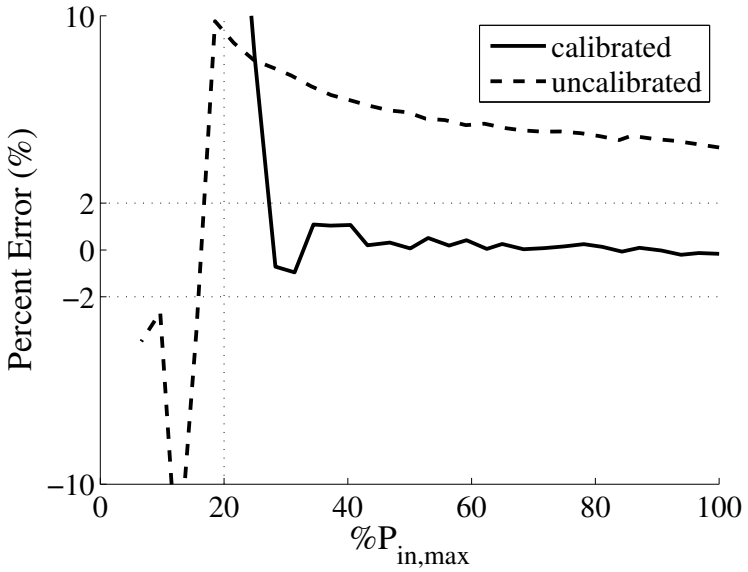
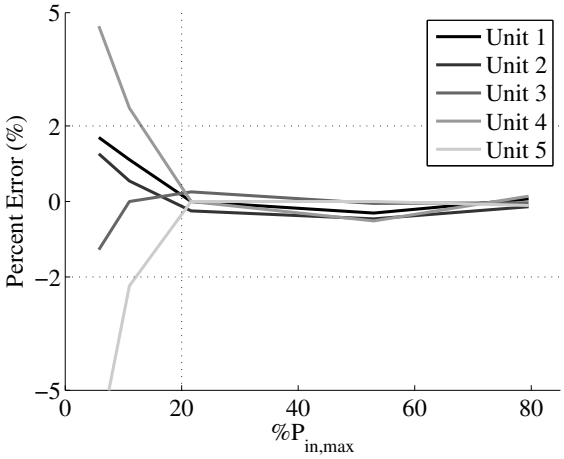


Figure 6.13: Power measurement percent error for the DNLC power measurement technique.

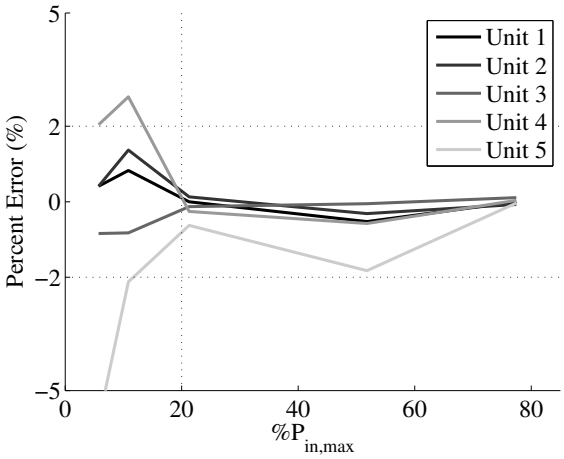
the collected input power measurement percent errors for an input voltage of 115V$_{rms}$, 220V$_{rms}$ and 260V$_{rms}$. In all cases the tested units provide a power measurement within the desired error bounds. Percent errors below the $0.2P_{in,max}$ limit are also quite low generally providing a bounded $\pm 5\%$ error at a power level near $0.05P_{in,max}$.

6.4 Chapter Summary

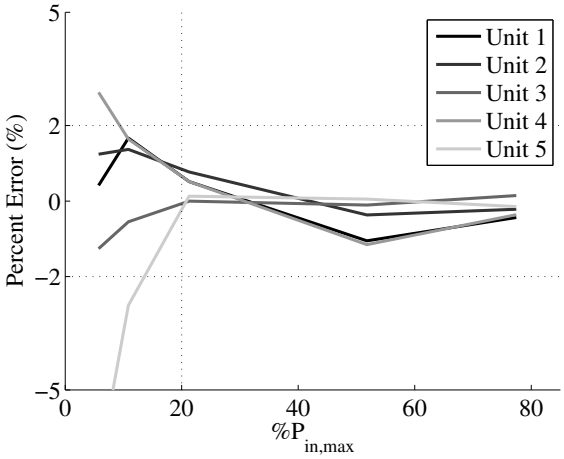
This chapter describes power measurement techniques using either data gathered for PFC stage control purposes or data available from downstream DC-DC controllers. A simple power measurement system is proposed for measuring power in a PFC rectifier with digital average current mode (DACM) control. An approach for input power measurement using digital nonlinear carrier control (DNLC) controller data has also been proposed and is shown to currently lack the required measurement accuracy over a wide power range regardless of calibration. Finally, it is shown how accurate input power measurements can also be attained if the PFC output dc current and voltage data are available. Both the DNLC and the output current sensing power measurement



(a) I_o sensing input power measurement percent error for $V_{line,rms} = 115V$.



(b) I_o sensing input power measurement percent error for $V_{line,rms} = 220V$.



(c) I_o sensing input power measurement percent error for $V_{line,rms} = 260V$.

Figure 6.14: Power measurement percent error for the I_o sensing power measurement technique.

approaches require the knowledge of converter efficiency for given operating points. In both cases, it is sufficient to perform characterization of average efficiency for a production unit type, and to store the efficiency correction data in a look-up table, thus reducing the need for per-unit calibration. Furthermore, the need for per-unit calibration could be completely eliminated if accurate current and voltage samples are available, which may be easier to accomplish using the output current sensing technique.

Chapter 7

Conclusions

The design, analysis and implementation of the digital non-linear carrier (DNLC) power factor correction (PFC) rectifier controller is the primary topic of this thesis. The DNLC PFC controller, like the analog non-linear carrier PFC controller [14], attains low harmonic input current shaping over a wide range of loads and input voltages without the need to sense the rectified input voltage. Additional characteristics of the DNLC PFC controlled boost rectifier provide significant advantages over other digital control approaches such as digital average current mode (DACM) control. These advantages include a relatively simple digital realization, the ability to avoid limit cycling of the outer voltage loop under constant power load conditions and reduced outer voltage loop bandwidth variation due to varying load power by implementing a single-comparator A/D (SCA/D) to sense the rectifier output voltage. Experimental results are shown for a 300W boost PFC rectifier. A list of the original contributions of this thesis is given below in Section 7.1. Possible directions for future research in the areas of DNLC PFC control, limit-cycling issues in PFC rectifiers, SCA/D implementations and input power measurement using sensed control data are outlined in Section 7.2.

7.1 Contributions:

- **Development of digital non-linear carrier (DNLC) PFC control**

  The basic DNLC PFC control law, given in (3.3), is derived using an input current shaping objective based on an effective emulated resistance at the PFC input and the quasi-static

approximated CCM voltage relationship between the boost converter input and output voltage. Analysis of the small-signal discrete-time current control loop shows stable operation of the DNLC PFC controller when the PFC operates in CCM during the entire line cycle. Modification of the basic control law, by the addition of a sensed current filter, gives an increased load range that results in stable CCM operation. At light loads the basic DNLC control law is modified to (3.10) to enable power control down to near zero load. The complete DNLC PFC controller shown in Fig. 3.4 incorporates many additional features such as a line synchronized voltage loop, an adaptive current sampling function to allow the use of a slower A/D and $\Sigma\Delta$ modulators to reduce hardware complexity.

- **Determination of no limit cycling conditions for digitally controlled PFC rectifiers:**

  Low frequency limit cycling in the power command signal of digitally controlled single-phase PFC rectifiers can increase the dc component and even harmonic current magnitudes of the input current. Two mechanisms that can cause low frequency limit cycling are identified: nonsynchronous sampling of the output voltage and quantization of the power command signal. Fig. 4.4(d) shows the concept of sampling the output voltage at a rate synchronous to twice the line frequency. This method of sampling allows for the implementation of an integral compensator in the outer voltage loop while still avoiding limit cycling due to output voltage sampling. The effects of quantization of the power command signal is investigated for both a DNLC and DACM controlled PFC rectifier. Utilizing the low-frequency small-signal model of a PFC rectifier, the control-to-output transfer functions of both controllers tested is summarized in Table 4.3 for either a resistive load or a constant power load. Finally, two no limit cycling conditions are prescribed that are functions of the PFC rectifier control-to-output transfer function dc gain and implemented voltage loop compensator gain parameters. This analysis predicts that the DACM controlled PFC rectifier will inherently limit cycle when the PFC rectifier supplies a high-efficiency, regulating DC-DC

downstream converter. The voltage loop compensator for a DNLC controlled PFC rectifier can be designed so that limit cycling is avoided even with a constant power load. This beneficial characteristic of the DNLC controlled PFC rectifier stems from the relation of the quantized power command signal to the rectifier's emulated input resistance and output voltage.

- **Development of a single analog comparator A/D (SCA/D) with power dependent gain characteristics:**

  A simplified PFC rectifier output voltage sensing analog-to-digital converter (A/D), shown in Fig. 5.1, is described in detail. Implementation of the SCA/D requires only an analog comparator with reference and a small amount of low-speed digital hardware. By sensing only the output of the analog comparator, the A/D reports the output error voltage and supplies a line synchronized clock at twice the line frequency for clocking of the outer voltage loop compensator. The unique power dependent gain characteristics of the SCA/D, shown in Fig. 5.6, provide a power feedforward gain correction for the dc loop gain of the outer voltage loop when the SCA/D is paired with a DNLC controlled PFC rectifier. The power feedforward mechanism reduces the variation in the dc loop gain as the power processing level of the PFC rectifier varies. Careful design of the outer voltage loop compensator and the SCA/D implementation results in improved load transient responses due to the increased voltage loop bandwidth compared to an identical PFC rectifier implementation with a traditional A/D.

- **Investigation of input power measurement techniques for DACM and DNLC controlled PFC rectifiers:**

  Input power measurement systems requiring no additional hardware or sensing are developed as shown in Fig. 6.3 and Fig. 6.4 for DACM and DNLC controlled PFC rectifiers respectively. For the DACM input power measurement technique analysis shows that the losses in the PFC's bridge rectifier and input filter can be compensated for by a simple

gain correction of the sensed inductor current as the bridge diode losses are dominant. The DNLC input power measurement technique requires compensation by the reciprocal of the converter efficiency. This correction is accomplished through the use of a look-up table (LUT) containing the average efficiency measurements for a particular power converter model. It is further shown that accurate input power measurements can only be obtained using the DNLC controlled PFC rectifier when the DNLC controller is operating under the non-modified current control law, (3.3). A simplified calibration routine is designed to reduce the calibration time. Experimental verification of the DACM input power measurement technique shows that adequately accurate input power measurements are possible using converter data originally purposed for PFC control. A third input power measurement technique relies on the availability of a measurement of the PFC's output current. This input power measurement technique also requires converter efficiency correction but does provide an accurate measurement of the PFC input power.

7.2 Directions for future research:

- **Modify DNLC PFC control for boundary conduction mode operation:**

  The DNLC PFC controller proposed in this thesis operates at a fixed switching frequency resulting in converter operation in CCM, DCM or a mix of both CCM and DCM during a input voltage half line cycle. Investigation into a mixed mode DNLC PFC controller that operates the converter in either CCM or boundary conduction mode (critical conduction mode) may produce a useful control technique for applications not requiring a fixed switching frequency. Operation in boundary conduction mode as opposed to DCM would likely improve the PFC rectifiers efficiency by enabling improved soft switching of the boost transistor during operation in boundary conduction mode.

- **Simplify inductor current sensing A/D requirements through inductor current estimation:**

Presently, digital PFC rectifier control techniques require that the inductor current be sensed at least once per converter switching period. To reduce the need for a high speed, medium resolution current sensing A/D, modified inductor current A/D structures, similar to the a single comparator A/D in Chapter 5, and inductor current estimation techniques could be developed. Of specific interest would be a inductor current estimation technique that is capable of adaptively tuning estimator parameters to mitigate circuit specific tolerances such as the inductor current value, gate drive delay asymmetry and input and output voltage sensing network gains.

- **Adaptively tune a PFC's outer voltage loop based on output voltage ripple magnitude and input power measurement:**

  The implementation of input power measurement techniques, like those discussed in Chapter 6, enables the development of adaptively tuned outer voltage loops. The gain of the outer voltage loop compensator could be adaptively tuned based on the averaged input power measured by the input power measurement block. Additionally, an estimation of the output capacitor value could be attained by measuring the approximate voltage ripple seen at the output and concurrently registering the average input power measurement. The estimation of the output capacitance value could then be used to approximate the outer voltage loop's bandwidth through modeling the system as an ideal rectifier. Tuning the bandwidth of the outer voltage loop would decrease the variation in line and load transient responses over a wide operating power range and for a wide range of output capacitance values.

- **Investigate the effects of downstream converter efficiency on outer voltage loop no limit cycling conditions:**

  Modeling of the outer voltage loop in PFC rectifiers in Chapter 4 reveals that DACM PFC controlled rectifiers will inherently limit cycle if they supply a constant power load. While modern downstream converters do tend to have both high efficiency and tight output regu-

lation, the characteristics of a constant power load, a more accurate input impedance model of the converters would increase the utility of the developed no-limit cycling conditions.

- **Modified SCA/D implementation mitigating A/D saturation and low power limit cycling:**

  The SCA/D developed in Chapter 5 implements an automatic power feedforward compensation mechanism that reduces the line and load transient variation over a wide operating power range. However, it is also shown that the SCA/D saturates for large transients and tends to limit cycle at low operating power levels. An implementation of the SCA/D using a traditional A/D structure could result in the desired power feedforward mechanism while eliminating A/D saturation effects. In steady-state the traditional A/D would be used as the single comparator in the SCA/D structure effectively generating the v_{comp} signal by detecting if the instantaneous output voltage is higher or lower than a quantization level. During transients the SCA/D based voltage loop would continue to operate unless the SCA/D saturated in which case the traditional A/D would be used to sense the output voltage directly. Also, by sensing the magnitude of the output voltage ripple with a traditional A/D, a conventional voltage loop could be used during low power operation in order to avoid low frequency limit cycling at the cost of reduced transient response due to the loss of the power feedforward mechanism inherent in the SCA/D architecture.

- **Develop a simple, low cost D/A for the implementation of hybrid PFC controller architectures:**

  Hybrid PFC controller structures require both A/D and D/A structures for implementation. The simple SCA/D from Chapter 5 provides a simple means to implement the A/D required for implementation of a digital outer voltage loop. The D/A that connects the output of the digital voltage loop and the analog current loop deserves investigation as well. Simple low-resolution current-steering D/As would likely be sufficient particularly with the implementation of increased time-modulated D/A resolution through the use of

$\Sigma\Delta$ modulator structures.

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Appendix A

DNLC Control Law Extension with Increased Current Filter Order

As mentioned in Section 3.1.1, the small-signal stability of a PFC current loop controlled by a DNLC PFC controller can be extended through the implementation of a sensed current filter. These filters and their resulting increased stability range for the DNLC PFC controlled current loop operating in CCM are discussed in detail in this Appendix.

The general form of the implemented sensed current filter is given by (3.8). Also, the small signal transfer functions of the boost power stage inductor current to duty cycle command and the basic DNLC PFC controller duty cycle command to inductor current are given by (3.5) and (3.6) respectively. The quasi-static approximation was previously used to relate the boost converter input and output voltage by the static DC/DC converter CCM conversion ratio. Even though the input voltage is changing, it is considered to change slowly enough that it can be assumed to be a large signal constant over the duration of a few converter switching periods. The same approximation is used here to justify the addition of a sensed current filter between the sensed inductor current and the input to the DNLC PFC controller. As the converter is assumed to be operating in steady state, the inclusion of the filter does not change the large signal operation of either the boost converter or the DNLC PFC controller as long as the DC gain of the sensed current filter is unity. The small-signal dynamics introduced by the inclusion of a sensed current filter do modify the small-signal characteristics of the current loop as a whole.

Fig. A.1 shows a diagram of the transfer functions included in the current loop gain calculation. As shown the sensed current filter is inserted at the input the DNLC PFC controller

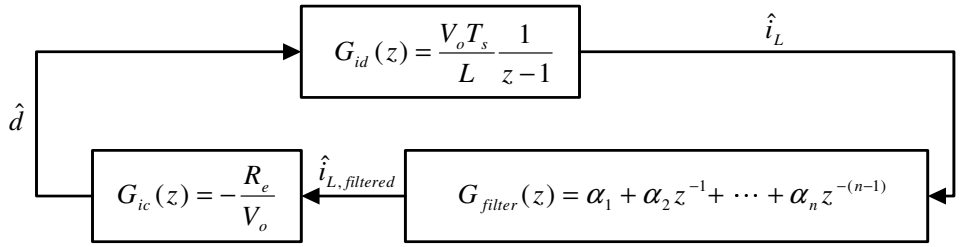


Figure A.1: Loop gain diagram of the DNLC PFC controller with an implemented sampled current filter.

(denoted by $G_{ic}(z)$). The characteristics of the sensed current filter are solely a function of the value of the filter coefficients (α's) and the order of the implemented filter. The purpose of the sensed current filter is to extend stable operating region of the DNLC PFC controlled current loop when the boost converter is operating in CCM. As discussed in Section 3.1.1 the basic DNLC PFC control law, (3.3), results in stable CCM operation as long as the converter operates in CCM during the entire line cycle. This corresponds to a maximum of $K_{crit} = 1$ where $K_{crit} = R_e T_s/2L$ which effectively limits the maximum magnitude of u to $2LK_{crit}/T_s V_o$. With the added dynamics of a sensed current filter the maximum stable K_{crit} can be increased as shown in Section 3.1.1 by the inclusion of a second order sensed current filter. It is important to note that the inclusion of the sensed current filter does not change the operating mode, CCM or DCM, of the current loop. The filters do however extend the range for stable CCM operation of the current loop below the power processing level where the current loop operates in CCM during the entire line cycle.

The optimal filter coefficients for sensed current filters up to 7^{th} order are shown in Table A.1. For the purposes of this study the optimal filter coefficients are the coefficients that give the broadest possible range of stable CCM operation for a given filter order. The filter coefficients for a given filter sum to one to maintain a unity DC filter gain. Also, inspection of Table A.1 shows that filter coefficients are monotonically decreasing in magnitude for higher order terms. These two characteristics of the sensed current filter coefficients were exploited to reduce the amount of effort required to solve for the optimal filter coefficients.

As mentioned in Section 3.1.1 the optimal filter coefficients were determined through the use

Table A.1: Extension of the K_{crit} stability range of the DNLC PFC controller using up to eight current filter coefficients.

K_{crit}		Current Filter Coefficients							
Ideal	Realized	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8
1.000	1.000	1.000	-	-	-	-	-	-	-
2.000	2.000	0.750	0.250	-	-	-	-	-	-
3.000	3.000	0.554	0.333	0.113	-	-	-	-	-
4.000	4.000	0.439	0.314	0.186	0.061	-	-	-	-
5.000	5.000	0.364	0.285	0.200	0.114	0.037	-	-	-
6.000	5.980	0.305	0.251	0.196	0.137	0.082	0.029	-	-
7.000	6.8821	0.260	0.214	0.180	0.143	0.104	0.070	0.028	-
8.000	7.436	0.238	0.199	0.169	0.133	0.108	0.078	0.053	0.024

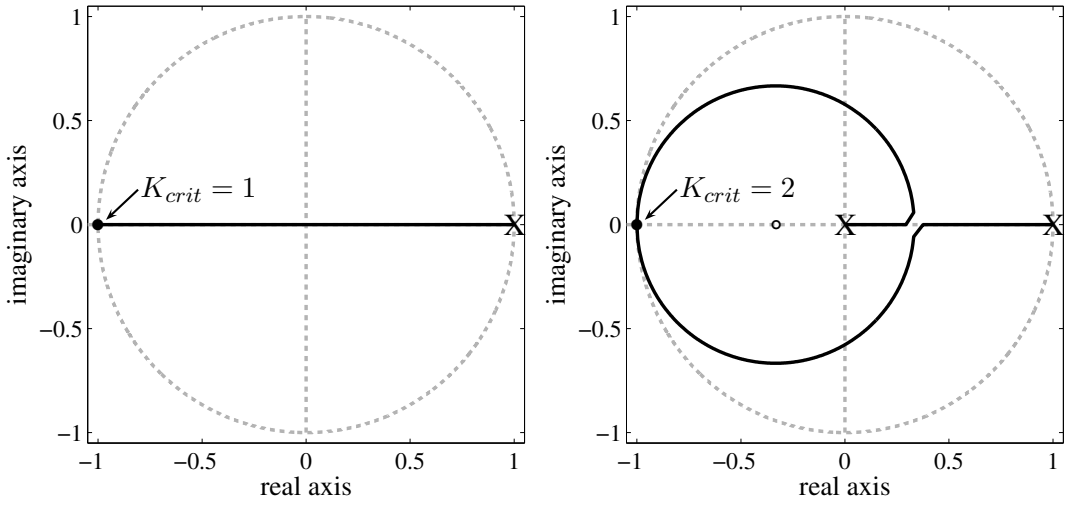
of a evolutionary algorithm. An evolutionary algorithm incorporates concepts commonly associated to the study of biological evolution such as fitness, hybridization, mutation and extinction. The fitness of a particular set of filter coefficients was determined by a root-locus analysis of the current loop with the implemented sensed current filter. A higher value of K_{crit} that resulted in a stable current loop indicated a higher fitness. Hybridization was accomplished by creating new sets of filter coefficients from two "parent" sets of coefficients. Half of the coefficients came from one parent and half came from the other parent. Additionally, selective hybridization was implemented that created hybridized coefficients from two high fitness sets of coefficients. Mutation was implemented by randomly modifying individual coefficients in the population. Finally, extinction was programmed by simply replacing low fitness sets of coefficients with new random sets of coefficients at regular intervals. An evolutionary algorithm was used because traditional numerical solving techniques failed to produce the desired results. This occurred because of the complex relationship between the filter coefficients and the resulting z-plane root-locus of the current loop. The limits of the programmed evolutionary algorithm are shown in the last three rows of Table A.1 where the expected maximum K_{crit} was not obtained. The algorithm did however produce filter coefficients that were near the expected result for the 5^{th} and 6^{th} order filters. The maximum K_{crit} obtained using the 7^{th} order filter is only 93% of the expected maximum K_{crit}.

The programmed evolutionary algorithm was used to solve the optimal coefficients for sensed

current filters up to seventh order. The root locus plots for DNLC PFC controlled current loops with implemented sensed current filters are shown in Figs. A.2 and A.3. The root locus plots for the basic DNLC PFC current loop and the first order sensed current filter loop are repeated from Section 3.1.1 in Fig. A.2 for completeness. In this figures the initial pole locations are denoted by an "X." Zero locations are also marked with the symbol "∘." The trajectory of conjugate poles is plotted using the same line style. The single real pole or pair of conjugate poles that eventually leaves the unit circle at a gain of K_{crit} is plotted as a solid black line.

Inspection of the root locus plots reveals that the maximum K_{crit} value is attained when either a single real pole traveling along the negative real axis crosses the unit circle at $z = -1$ or a pair of conjugate poles meets at $z = -1$ and splits into two real poles. Other closed loop poles seen at higher filter orders from conjugate pairs and have trajectories that start at the origin, run tangent to the unit circle at one K_{crit} value, and then approach system conjugate zeros at higher gains. The closed loop pole at $z = 1$, due to the plant integrator, is continuously present in all root-locus plots.

The utility of implementing a current sense filter to extend the stable CCM operating range is demonstrated in Chapter 3. Further extension of the DNLC PFC controller through the use of higher order sensed current filters comes at the cost of implementing the sensed current filter with accurate coefficients. Clearly the coefficients for the two coefficient, first order filter, are conducive to simple digital implementation. However, beyond the first order filter the required filter coefficients become increasingly difficult to accurately realize. Additionally, the benefit of increasing the range of stable CCM operation quickly diminishes as operating power decreases as the converter operates in DCM during an increasing portion of the half line period. Implementing a sensed current filter does have other advantages. These include improved noise immunity and improved current loop behavior when transition between CCM and DCM. The amount of sensed current filtering that would achieve these advantages is certainly dependent on application specifics.



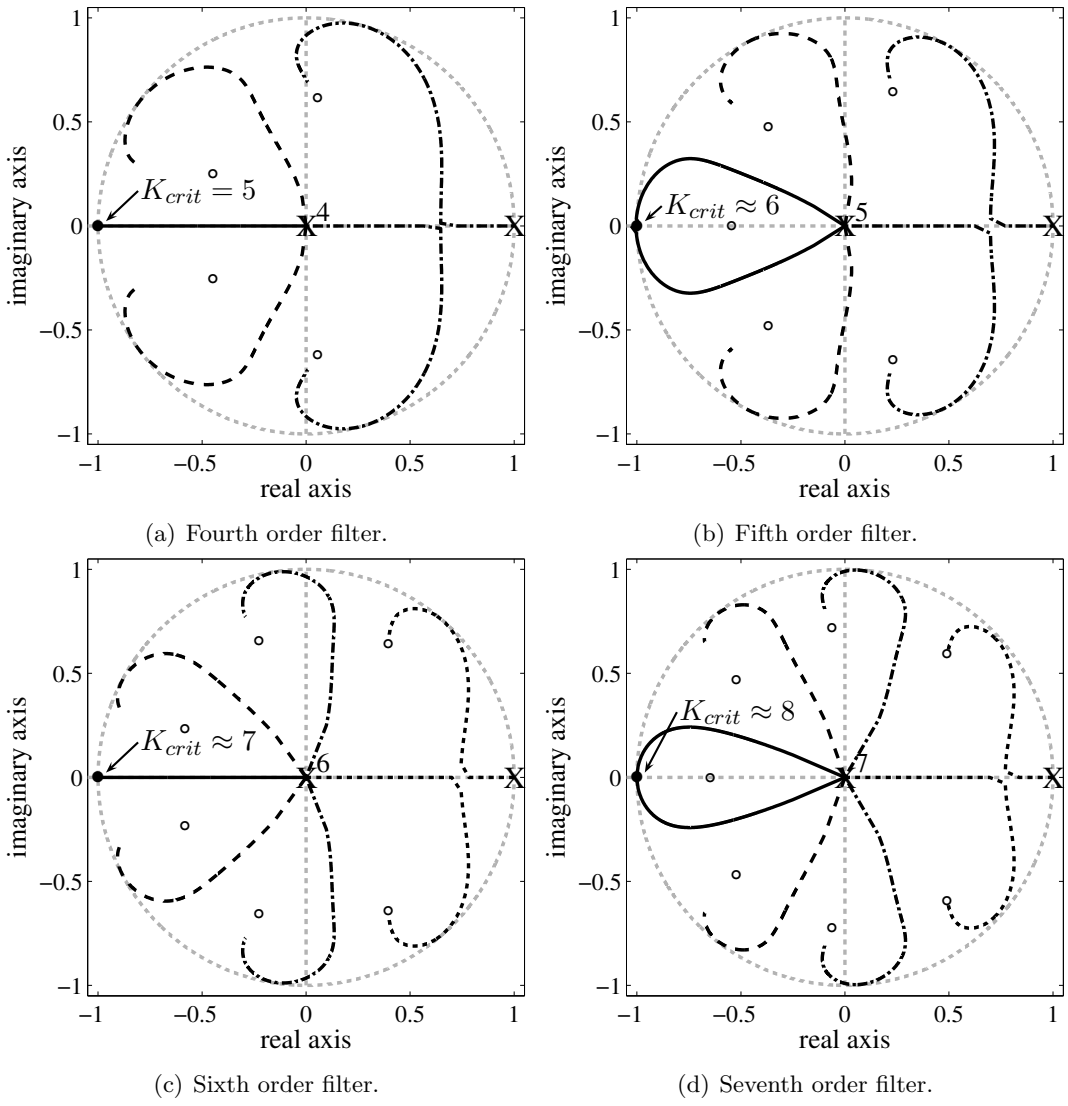
(a) Basic current control law.

(b) First order filter.

(c) Second order filter.

(d) Third order filter.

Figure A.2: Root loci of DNLC PFC controlled current loops with current filters up to 3$^{\text{rd}}$ order.



(a) Fourth order filter.

(b) Fifth order filter.

(c) Sixth order filter.

(d) Seventh order filter.

Figure A.3: Root loci of DNLC PFC controlled current loops with current filters from 4^{th} to 7^{th} order.